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Bursts of Pulses for Time Domain Large Signal Measurements

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***Abstract*—An enhanced pulsed mode for RF measurements based on synchronized repetitive signals is proposed, with the unique capability to manage repetitive sets of pulses and consequently to investigate the pulse-to-pulse behavior of high power active devices. This new technology is applied to a sampler-based NVNA (Nonlinear Vector Network Analyzers), without any dynamical losses. Burst of Pulses measurements of high power AlGaN/GaN transistors are performed in a multi-harmonic passive load-pull environment. Time domain waveforms and S21 pulse-to-pulse phase within the burst are acquired and discussed.**

I. INTRODUCTION

The low frequency memory effects taking place into high power active devices are now one of the most critical points for the design of RF power amplifiers with demanding specifications in terms of linearity and power efficiency. GaN devices are still very prone to such long term effects, the trapping and thermal effects. In a general manner, modulated signals are affected by such dynamical nonlinearities. In the particular case of radars, the pulse-to-pulse behavior of the device is modified by the recent device history. Practically speaking, this means the gain and phase transfer characteristics of the power amplifier can depend on the pulse position or pulse number.

PIV (Pulsed I(V)) and pulsed RF measurement techniques have already proven their efficiency for the characterization of high power devices [1][2]. A pulsed mode for the LSNA has been described in [3], with a technique that keeps the dynamical range of the measurement system, even for very long duty cycles [4] [5]. The burst of pulses measurement mode is a significant improvement of that previous work. This paper mainly describes the technique used to get such measurements without any dynamical losses.

II. RF MEASUREMENT PRINCIPLE FOR BURSTS OF PULSES

The sampler-based NVNA synchronized down-conversion results in an IF signal that contains an image of the RF signal, including its harmonic frequencies due to nonlinearities [6]. The ADC acquisition of that IF signal is usually not constrained to a particular setting, providing the relevant frequencies witch are in the scope of the FFT performed after the ADC data acquisition. In the case of bursts of pulses RF signals, we propose to phase-lock and to set very accurately the ADC frequency. The ADC frequency choice depends on the IF frequencies of interest, of the pulse period, of the burst period, of the number of samples per pulse, and the number of FFT points.

The Fig. 1 shows the effect on ADC samples of well-chosen ADC frequency and other parameters. We propose here bursts of 2 pulses, the measurements are taken during the second pulse, and 6 ADC samples values are acquired during each considered pulses. Note that, for simplification purpose, the IF signals here is a sine, without harmonics. The phase of the last ADC sample taken during the first measurement shot is exactly followed by the phase of the first sample of the next shot. An easy check-up of that approach precision consists in looking at the IF signal FFT, with no existing leakage around the expected frequency bins. As an obvious consequence, the data record obtained is equivalent to a CW record, and can be managed by regular NVNA algorithms (FFT, RF absolute calibration corrections, FFT^{-1}...).

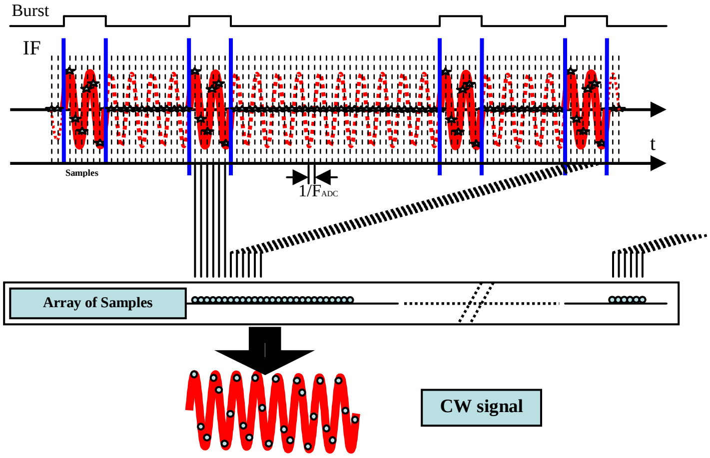

Fig.1 Synchronized ADCs for Bursts of Pulses, 2 pulses each burst, measurements taken during the second pulses, 6 samples each measured pulse

III. HARDWARE DETAILS

This approach of a synchronized acquisition of bursts of pulses requires several high precision phase-locked clocks. A simplified hardware example schema is proposed at Fig 2. Three high precision synthesizers are driven by the same high stability clock: the main RF source, the RF samplers clock (FracN1), the ADC clock (FracN2).

The pulse and burst triggers are derived from the ADC clock by the means of 4 programmable digital counters/dividers. The outputs of these counters are driving the pulse modulator of the RF source, the ADC trigger, and the optional PIV (Pulsed I(V)) subsystem. The delayed burst trigger (DBT) allows taking measurements at any position within the bursts, ie choose an arbitrary pulse and an arbitrary position inside this pulse. This signal can also trigger the optional PIV acquisition hardware.

This improvement of NVNA's capabilities has been tested successfully with two different NVNA equipments:

-The classical MTA-based LSNA (sold by Maury/NMDG). We have make use of the embedded PC we have previously added ourselves in that system [7] in order to control the FracN2 synthesizer and our counters/dividers PCB.

-The new VTD receiver SWAP X-402. This equipment, with a very recent design, disposes internally of all the required hardware parts for the bursts of pulses mode, and its faster IF and ADC circuitry allows shorter pulses.

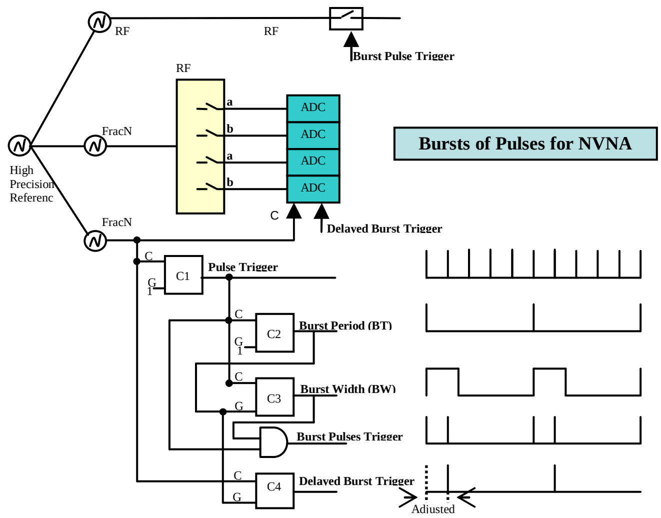

Fig. 2: Clocks and triggers for bursts of pulses

As all the clocks are derived form the same reference, and with exact computation of all the frequencies, this approach does not exhibit new specific short term jitter problems. The high precision reference has to be good enough to avoid long-term jitters; very high duty cycles have already been measured successfully and reported with a simplified approach (pulses only) [4].

IV. Example of settings

We propose a complete system setting for a measurement. The RF fundamental frequency is 2 GHz, and 10 harmonic frequencies are considered, up to 20 GHz.

The RF sampling frequency (FracN1) is 19,999,000 Hz. Then the IF image of the 2 GHz RF signal is 100 KHz, it's 200 KHz for the 4 GHz frequency, 300 KHz for 6 GHz….

The ADC frequency (FracN2) is 12.8 MHz, the time between 2 ADC samples is 78.125 ns. The FFT size is 16384 samples, then the FFT bin for the 2GHz is 128, it's 256 for 2 GHz, 384 for 6 GHz…

We propose a pulse width of 1 µs; a pulse period of 10 µs and a burst period of 100 µs. We are taking two pulses in the burst period. It means the C1 divider (Fig. 2) contains 128, the C3 contains 2 and the C2 contains 10. With this configuration we get 2 pulses at the burst pulse trigger (BPT) signal for each period of the burst trigger (BT).

During each pulse to consider for data acquisition, 4 ADC samples are taken (this is done synchronously for each measurement channel). As a consequence, we need to consider 4096 bursts in order to dispose of 16384 ADC samples. The complete measurement takes approximately 410 ms.

As one can notice, these clock and counter settings must fulfill several severe numerical requirements in order to produce no measurement leakage. We have written software to compute these settings: it inputs the RF fundamental frequency, the pulses and burst requirements and proposes the nearest suitable configuration.

V. Measurements results

We will now demonstrate our capabilities to measure burst of pulses with the described NVNA stroboscopic time domain approach. We will mainly show here the consistency of time domain measurements performed at both ports of a microwave power transistor.

The measurements are performed on an AlGaN/GaN HEMT from Alcatel-Thales III-V Lab with 4×200µm gate width. For all measurements, the fundamental frequency is 4 GHz, 5 harmonic frequencies are measured up to 20 GHz. The gate voltage is DC driven with V_{GS}=-5.9V, but the drain voltage is pulsed from V_{DS0}=0V outside of the pulses to V_{DSi}=25V inside the pulses. The device load impedance is set to (27-j6) Ω at 4GHz, this point is optimized for output power, and no optimization has been performed at harmonic frequencies. The power sweeps figures are stopped as soon as the device exhibits 4 dB of gain compression.

As shown on Fig.3, we apply 1µs pulses, with a pulse period of 10µs and a burst period of 100µs. During each burst, 3 pulses are applied. The measurements can be taken at any time, but we will only consider here measurements taken during the first and the third pulses. For each measurement trigger, only 2 ADC samples are considered, the ADC period is 71.0227 ns, and the FFT size is 16384. It means the IF measurement duration is roughly 142ns. Thus the real measurement duty cycle is 142ns/100µs, i.e. 0.142%, and the total measurement duration is 0.8192s.

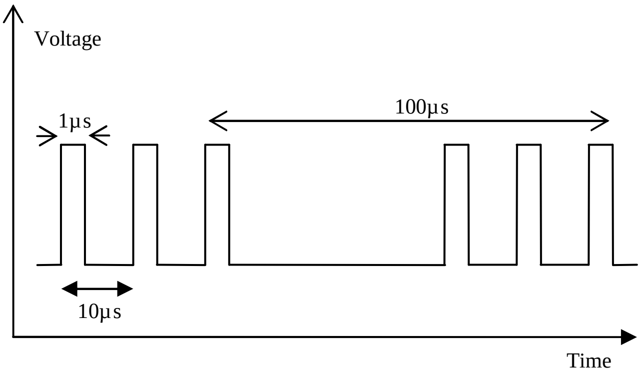

Fig. 3: The pulse and burst configuration for the measurements

The Fig.4.a and Fig.4.b present the time domain waveforms acquired at the output planes (probe tips) of the transistor during the first pulse of each bursts.

The Fig.5.a and Fig.5.b show to the time domain waveforms at the output of the DUT for the same conditions and settings, but the measurement are taken during the third pulse of each burst. This change of measurement timing is simply done with the setting of the C4 counter driving the DBT signal.

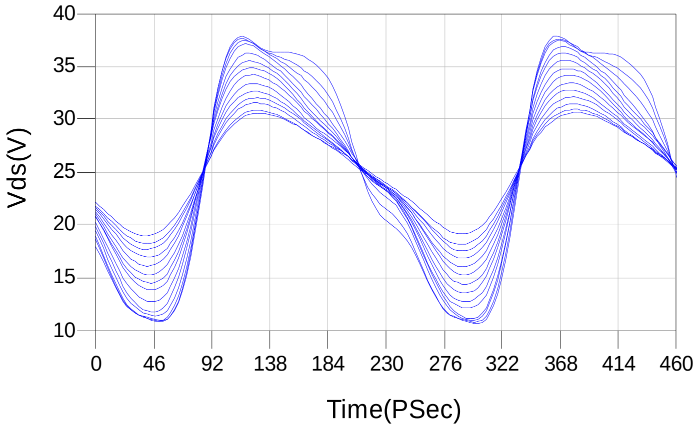

Fig. 4.a Drain voltage versus time during the first pulse, power sweep

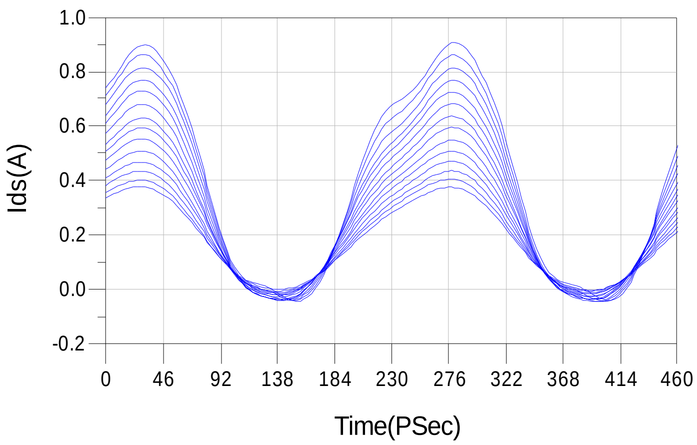

Fig. 4.b Drain current versus time during the first pulse, power sweep

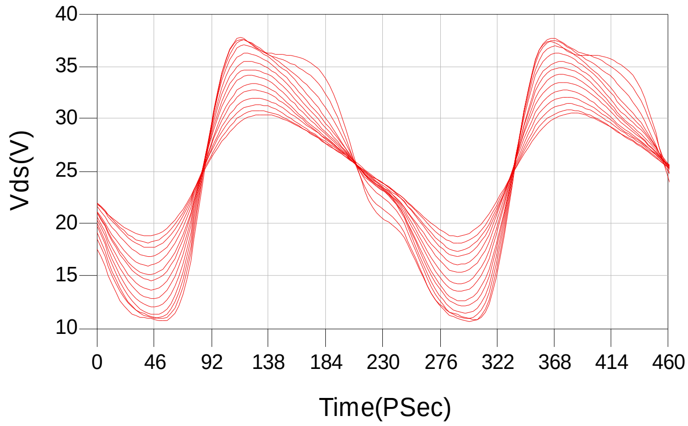

Fig. 5.a Drain voltage versus time during the third pulse, power sweep

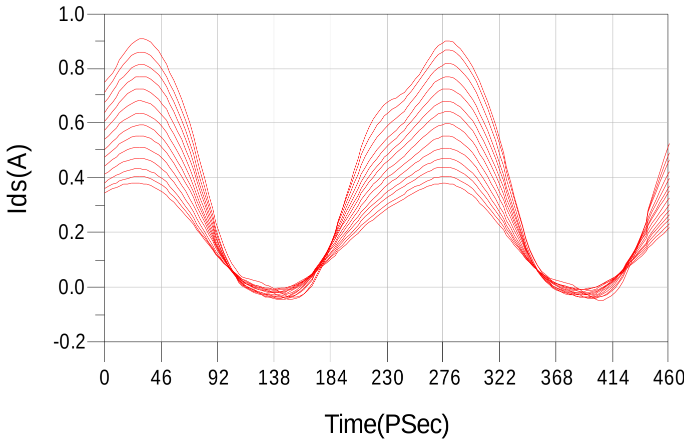

Fig. 5.b Drain current versus time during the third pulse, power sweep

This first set of measurements does not show any noticeable discrepancy between the two measurement epochs. As we do not have driven the transistor under test close to its limits (V_{DS} is not very high, the dissipated power is still low), it does not exhibits many memory effects. In fact, this is exactly the situation we were looking for now, in order to check our new measurement approach. We first wanted to show that the measurement accuracy and consistency is not reduced with this new bursts-of-pulses mode.

A more sensitive test of this measurement consistency consists in looking at the B2/A1 phase. This is roughly the phase of the transistor gain S21 (but with a calibration at the probe tips). As this phase parameter is of great importance for radar applications, we compare with our transistor the phase of the gain during the first and the third pulse of the burst. We have done this comparison for the fundamental frequency (4 GHz) at Fig.6 and for the first harmonic frequency (8 GHz) at Fig.7.

It turns out that the phases measured during the first and the third pulse are very similar, the difference is smaller than 0.2 degrees as soon as the input power is larger than -12 dBm. This nice result does not mean the absolute values of the phases are so accurate; they still depend on the calibration quality and reference plane definitions. But the comparison of both pulses, with all the other settings still identical, indicates the quality of the phase shift measurement we can achieve with our set-up. This demonstrates our burst of pulses measurement capabilities without dynamical losses. This result also confirms that our DUT, biased and driven as indicated, does not exhibit significant memories in the range of 20 µs.

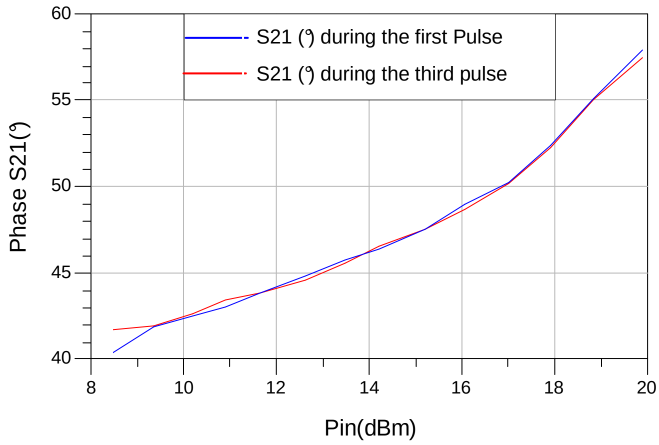

Fig. 6 S21 phase versus input power @ f0, first pulse and third pulse

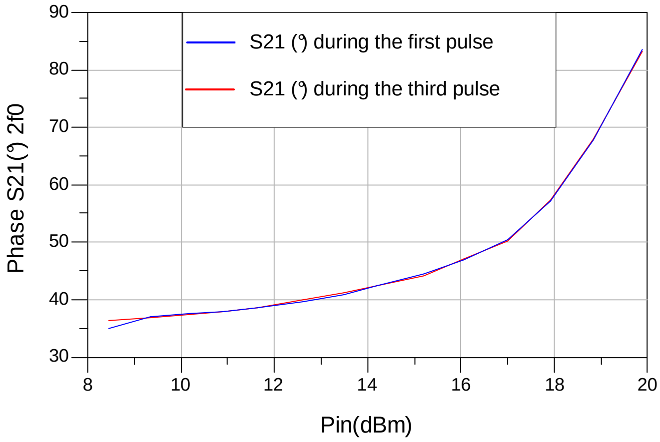

Fig. 7 S21 phase versus input power @2f0, first pulse and third pulse

Our next work with this new setup will be to measure in severe condition very high power transistors or power amplifiers ICs (we can handle up to 20 Watts for on-wafer DUT and 100 Watts for connectorized devices). We will be able to change the settings (pulse period, pulse duration, burst period, power, PIV, match…) in order to look for memory effects. We suppose we will be able to demonstrate the effects of DUT memories on pulsed and modulated signals, especially radar signals.

VI. Conclusion

We propose a new measurement mode for sampler-based NVNAs with enhanced pulses and bursts capabilities in order to investigate the effects of DUT memories in realistic conditions; this approach can be combined with a PIV biasing system. We can measure accurately the time domain waveforms and the pulse-to-pulse phase shifts of active devices when applying radar-like signals.

Acknowledgment

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