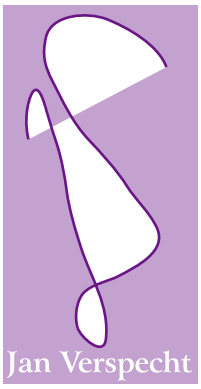

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Introduction to Measurements for Power Transistor Characterization

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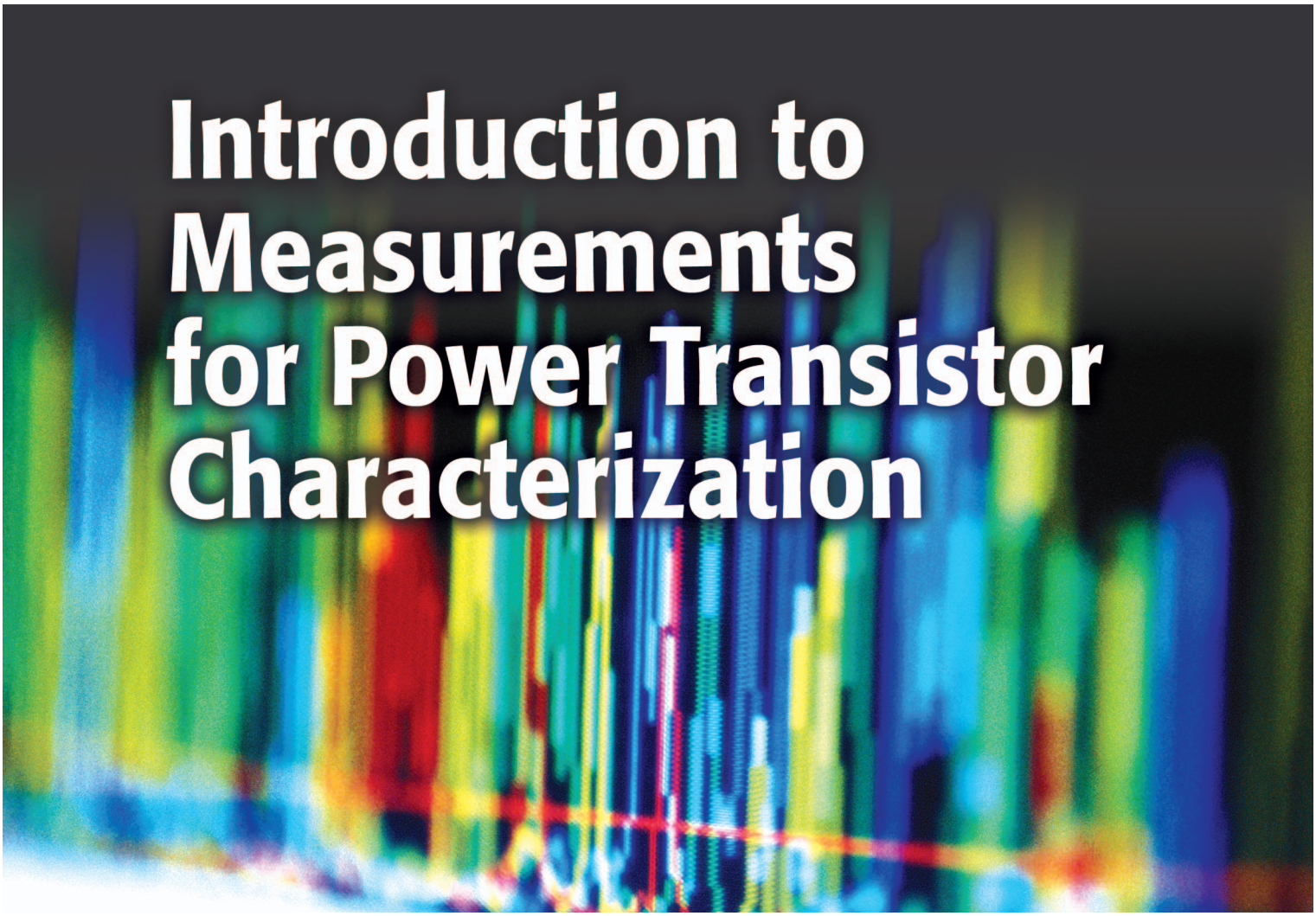

Fabien De Groote, Jean-Pierre Teyssier, Tony Gasseling, Olivier Jardel, and Jan Verspecht

In this article, we will introduce you to measurements for power transistor characterization: why they matter, why they are such a complicated, highly specialized field, and where we think the technology of power transistor characterization is headed. To accomplish this goal, we will use simple examples and explanations, at the risk of oversimplifying the matter. For those individuals who want to dive deeper into the subject, we provide plenty of references. Note that the list of references is far from complete, but we are convinced that it is a good starting point. If you are already an expert in the field, there may be little chance that you will learn new things; nevertheless, we hope that you can still enjoy the reading. Please note that we restrict ourselves as much as possible to the characterization aspects, and only refer to modeling aspects if they are useful in the context of transistor characterization.

Why Power Transistor Characterization Matters

The microwave power amplifier is the workhorse of the wireless communications industry. It converts simple dc power into complex radio

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waves that travel through space to enable wireless communication. Designing power amplifiers is a daunting task [1]. One reason is that many strict regulations apply—for example, limitations on the creation of undesired spectral components [often quantified by adjacent-channel power ratio (ACPR)] and limitations on the maximum allowable distortion of the information carried by the radio waves [often quantified by error vector magnitude (EVM)]. These regulations make a lot of sense since the spectrum gets increasingly crowded and there is a need to prevent interference caused by undesired spectral components generated by your neighbor's power amplifier, while at the same time making sure that the information that you get while talking to your partner is undistorted. As it turns out, you don't need a lot of distortion to turn "I do" into "I don't," with potentially disastrous consequences. But there is another reason why the design of power amplifiers is daunting. Whereas the power amplifier is the workhorse of the wireless communications industry, the power transistor inside the power amplifier is its problem child. In other words, power transistors often don't behave the way the designer expects. It is the responsibility of the power amplifier designer to make sure that he or she can integrate the problem child transistor into a well-behaved power amplifier that obeys strict regulations. If you are a parent (or a problem child) yourself, you will certainly understand the issue.

Fortunately, the designer is not alone since he or she can get help from the transistor modeler. A transistor modeler is someone who interacts with the transistor through a multitude of experiments and who extracts a mathematical model from the measured data. This model describes how the transistor behaves under a wide range of excitation signals and operating conditions. This mathematical model is nothing more than a description of the relationship between the voltage waveforms and the current waveforms as they appear at the transistor terminals. The transistor model is then used by the designer in a simulator to predict the performance of any amplifier circuit containing the modeled transistor, even before the amplifier is actually built. The designer can quickly optimize the parameters of his or her design in the simulator to make sure that the design will meet the desired specifications. Only then will a prototype of the amplifier be built and tested. If the model is a good one, the prototype amplifier will meet the specs and the designer can proudly inform his or her manager that the design project is completed! If the designer is lucky, he or she may even get a raise. If the model is not a good one, however, the prototype amplifier will not meet the specs. But that is not all. If the model is bad, the designer may have no clue at all about what to do to improve the design and the only alternative is often an inefficient trial-and-error design approach. Needless to say, under these circumstances, the designer needs to be really, really lucky to get a raise. The above clearly illustrates the value of a good transistor model as it greatly influences the time to market of any power amplifier design.

So what does it take to get a good model? The transistor modeler starts by gathering knowledge about the physical parameters of the transistor: doping profiles, physical dimensions, number of fingers, etc. This information is sufficient to get a rough idea about the operating region of the transistor—for example, maximum voltage or current, maximum power dissipation, or breakdown voltage. The physical information is also sufficient to get an idea of the mathematical structure of the relationship between the voltage and current waveforms. For example, knowing that the transistor is a field-effect transistor (FET) is sufficient information to know that the drain current is mainly a function of the gate voltage, whereas knowing that the transistor is a bipolar junction transistor (BJT) is sufficient information to know that that the collector current is mainly a function of the base current.

Next, the transistor modeler applies a variety of signals to the transistor terminals and measures quantities that are related to the voltage and current waveforms. The quantities that are measured can be the instantaneous values of the voltages and currents themselves, but can also be other derived quantities like *S*-parameters, or the time averaged values of the voltages and currents. The trick is to apply a minimum number of excitation signals that allows the modeler to determine all unknown parameters of the model. This is called the problem of experiment design. Once the modeler has determined all the parameters of the model, he or she will try to find a mathematical relationship between the voltage waveforms and current waveforms that is consistent with the measured quantities. If the assumed mathematical structure of the model is complete, the model will be capable of predicting the relationship between the voltage waveforms and current waveforms under a range of excitation signals that is much wider than the range of excitation signals used during the model extraction.

If in doubt, the modeler will verify assumptions on the mathematical structure of the model by performing model validation experiments. The idea of model validation is to provide excitation signals that are as close as possible to the signals that will be seen by the transistor in a final application, and to verify whether the model can predict the measured results. If the model succeeds in the validation test, the modeler is ready to transfer the model to the designer. Note that the signals that are used for model extraction are usually much different from the signals that the transistor will see in a final application.

The process of designing the experiments and performing the transistor measurements, for the purpose of model extraction as well as model validation, is what we call "transistor characterization." It is clear from the above discussion that good power transistor characterization is an indispensable tool for building

good transistor models. To summarize, power transistor characterization matters because it is vital for building good transistor models, which are necessary for designing good amplifiers capable of ensuring clear conversations with our partners on our mobile phones.

Why Microwave Power Transistor Characterization People Arrive Late at Parties

One may wonder why microwave power transistor characterization is so difficult. Many engineers probably remember characterizing simple BJTs in the student lab. It is really easy. One injects a current I_B into the base of the junction transistor, applies a voltage V_{CE} across the collector and emitter, and simply measures the corresponding collector current I_C and the corresponding base-emitter voltage V_{BE}. This measurement is then repeated for a whole range of base currents and collector voltages. If performed with enough resolution, this process results in two measured, two-dimensional (2-D) functions $F_{BE}(.,.)$ and $F_C(.,.)$ that describe V_{BE} and I_C as a function of V_{CE} and I_B

$$V_{BE} = F_{BE}(V_{CE}, I_B) \tag{1}$$

$$I_C = F_C(V_{CE}, I_B)\,. \tag{2}$$

If we are dealing with an FET, we do a similar set of measurements whereby we apply gate voltages (V_G) and drain voltages (V_D), and we measure the corresponding gate current (I_G) and drain current (I_D). This results in two measured, 2-D functions $F_G(.,.)$ and $F_D(.,.)$ that describe I_G and I_D as a function of V_G and V_D

$$I_G = F_G(V_G, V_D) \tag{3}$$

$$I_D = F_D(V_G, V_D)\,. \tag{4}$$

And we are done—the transistor is characterized and we can go party. We only need to send the measured data to the transistor modeler, who constructs an equivalent electrical network that behaves according to (1) and (2). This equivalent electrical network is the actual transistor model. It runs in the simulator and can be used by the designer to optimize his design. Note that, since this article is about transistor characterization, we will not further elaborate on the modeling process itself.

So, why wouldn't that kind of data be sufficient to model a microwave power transistor? In other words, why is it that people who characterize microwave power transistors are often still measuring at a time when many others are partying? The answer is actually pretty simple: this is first of all because of the "microwave," and secondly because of the "power."

The Microwave Aspect

We will first elaborate on the "microwave" aspect. If we were to explain to a layperson what microwave signals are [2], we could probably get away with saying that these are electrical signals that vary incredibly fast. In fact, light travels less than a foot during the time it takes for these signals to go up and down once. So, how is this related to the fact that the microwave transistor modeler is not satisfied if we provide him/her with the same measurements as before? Why can't he or she just tell the designer to use the simulator to apply such rapidly varying electrical voltage signals $V_G(t)$ and $V_D(t)$ to the simple extracted FET model of (3) and (4) to predict the corresponding currents $I_D(t)$ and $I_G(t)$?

$$I_G(t) = F_G(V_G(t), V_D(t))\,? \tag{5}$$

$$I_D(t) = F_D(V_G(t), V_D(t))\,? \tag{6}$$

The answer is that the microwave voltage signal varies so fast that even a relatively small capacitor, inevitably present in any FET device, will start drawing a significant capacitive current that will partly show up at the terminals. In a similar manner, any relatively small inductance, inevitably present in any transistor layout, will start generating a significant inductive voltage that will partly show up at the transistor terminals. This implies that any model, in order to accurately predict the terminal currents, will need to contain capacitive as well as inductive elements. Assume for a moment that our modeler adds capacitive currents to the model as illustrated by (3) and (4). The result, which is actually the fundamental idea of the well-known Root modeling approach [3], is

$$I_G(t) = F_G(V_G(t), V_D(t)) + \frac{dQ_G(V_G(t), V_D(t))}{dt}\,, \tag{7}$$

$$I_D(t) = F_D(V_G(t), V_D(t)) + \frac{dQ_D(V_G(t), V_D(t))}{dt}\,. \tag{8}$$

Note that this is certainly not the only way that a modeler would add capacitive currents, but we restrict ourselves to this case because it is great for educational purposes while at the same time actually being regularly used in industry. The functions $Q_G(.)$ and $Q_D(.)$ represent the charge storage that occurs in parallel with the FET transistor terminals. Note that the actual Root model is somewhat more sophisticated, and that we are using a simplified version for the sake of illustrating the transistor characterization issues rather than diving into modeling issues.

The modeler will now tell you that the dc data that you provided is sufficient to model the $F_G(.)$ and $F_D(.)$ parts, but contains no information at all on the charge storage functions $Q_G(.)$ and $Q_D(.)$, since we have only measured at constant V_G and V_D. In other words, during our measurements, the capacitive current is always equal to zero. Note that a similar conclusion not only applies to the Root model, but in general to all models containing capacitive and inductive elements: one can simply not extract any information on inductors and capacitors from dc measurements. The question then becomes the following: What kind of characterization

measurements can be performed to enable the modeler to characterize these capacitors and the inductors in the model? It is clear that to extract that information we actually need to apply microwave signals to the transistor terminals and measure the relationship between the voltage and current waveforms.

If we operate in the microwave domain, *S*-parameter measurements are obviously the measurement technique of choice. The idea is then to apply a dc gate voltage V_{G0} and a dc drain voltage V_{D0} and to measure the corresponding gate current I_{G0}, drain current $I_{D0,}$ and the corresponding *S*-parameters. This is then repeated across the entire (V_G, V_D) operating range of the transistor. Needless to say that this process results in a lot of data: two 2-D functions $F_G(.,.)$ and $F_D(.,.)$ and four bias-dependent *S*-parameter functions $S_{11}(.,.)$, $S_{12}(.,.)$, $S_{22}(.,.)$ and $S_{21}(.,.)$. It is then the task of the modeler to identify all of the inductors and capacitors in the model by analyzing the additional *S*-parameter data. The fact that the *S*-parameter measurements contain sufficient data to extract the inductive and capacitive elements of the model can be demonstrated by looking at the simplified Root model as described by (7) and (8). Consider that one applies a gate voltage of V_{G0} and a drain voltage of V_{DO} to the FET. During the *S*-parameter measurement, a small microwave signal will excite the device, resulting in fast voltage and current variations. Let us denote these variations by $v_g(t)$ for the gate voltage variation, $v_d(t)$ for the drain voltage variation, $i_g(t)$ for the gate current variation, and $i_d(t)$ for the drain voltage variation. We can then write

$$I_{G0} + i_g(t) = F_G(V_{G0} + v_g(t), V_{D0} + v_d(t)) + \frac{dQ_G(V_{G0} + v_g(t), V_{D0} + v_d(t))}{dt}, \tag{9}$$

$$I_{D0} + i_d(t) = F_D(V_{G0} + v_g(t), V_{D0} + v_d(t)) + \frac{dQ_D(V_{G0} + v_g(t), V_{D0} + v_d(t))}{dt}. \tag{10}$$

Since the time-varying deviations are small, the above equations reduce to

$$i_g(t) = \frac{\partial F_G}{\partial V_g} v_g(t) + \frac{\partial F_G}{\partial V_d} v_d(t) + \frac{\partial Q_G}{\partial V_g} \frac{dv_g(t)}{dt} + \frac{\partial Q_G}{\partial V_d} \frac{dv_d(t)}{dt}. \tag{11}$$

$$i_d(t) = \frac{\partial F_D}{\partial V_g} v_g(t) + \frac{\partial F_D}{\partial V_d} v_d(t) + \frac{\partial Q_D}{\partial V_g} \frac{dv_g(t)}{dt} + \frac{\partial Q_D}{\partial V_d} \frac{dv_d(t)}{dt}. \tag{12}$$

Note that each of the partial derivates in the above equation is constant during each *S*-parameter measurement and is evaluated in (V_{G0}, V_{DO}). Next one converts (11) and (12) to the frequency domain. The result is

$$I_g(\omega) = \left(\frac{\partial F_G}{\partial V_g} + \frac{\partial Q_G}{\partial V_g} j\omega\right) V_g(\omega) + \left(\frac{\partial F_G}{\partial V_d} + \frac{\partial Q_G}{\partial V_d} j\omega\right) V_d(\omega), \tag{13}$$

$$I_d(\omega) = \left(\frac{\partial F_D}{\partial V_g} + \frac{\partial Q_D}{\partial V_g} j\omega\right) V_g(\omega) + \left(\frac{\partial F_D}{\partial V_d} + \frac{\partial Q_D}{\partial V_d} j\omega\right) V_d(\omega). \tag{14}$$

Equations (13) and (14) reveal that there is a simple relationship between the partial derivatives of the charge storage functions and the imaginary part of the *Y*-parameters. Assuming that port 1 is connected to the gate of our transistor and port 2 is connected to the drain, one finds that

$$\mathrm{Im}Y_{11}(\omega) = \frac{\partial Q_G}{\partial V_g}\omega, \tag{15}$$

$$\mathrm{Im}Y_{12}(\omega) = \frac{\partial Q_G}{\partial V_d}\omega, \tag{16}$$

$$\mathrm{Im}Y_{21}(\omega) = \frac{\partial Q_D}{\partial V_g}\omega, \tag{17}$$

$$\mathrm{Im}Y_{22}(\omega) = \frac{\partial Q_D}{\partial V_d}\omega. \tag{18}$$

The idea is then to measure bias-dependent *S*-parameters and convert the *S*-parameters into *Y*-parameters. As shown by (15)–(18), the bias-dependent *Y*-parameters contain information on the partial derivatives of the charge storage functions. The modeler integrates the measured *Y*-parameters and can reconstruct the unknown charge storage functions. It is not hard to imagine that a similar approach will also give you information on the inductive effects, rather than the capacitive effects. The essential conclusion is that bias-dependent *S*-parameters are necessary for determining the capacitive and inductive elements of the transistor. This principle does not only apply to the Root model, but in general applies to all modeling techniques.

The Power Aspect: Many Amplifiers Are as Much Electrical Heater as They Are Signal Amplifier

So we have performed a lot of measurements and we have succeeded in gathering a lot of data: two 2-D functions $F_G(.,.)$ and $F_D(.,.)$ and four bias-dependent *S*-parameter functions $S_{11}(.,.)$, $S_{12}(.,.)$, $S_{22}(.,.)$ and $S_{21}(.,.)$. As stated before, this data should be sufficient

to identify the static voltage and current parts of the transistor model, as well as all of the inductive and capacitive parts. In short, we can state that such a set of measurements should be sufficient to characterize all of the pure electronic effects that are happening inside the transistor. So why isn't the modeler happy with this data? The answer is that the power transistor behavior is not just described by pure electronics. As stated earlier, the power transistor is the component that converts a lot of dc power into a lot of microwave power. Unfortunately, the power transistor does not only convert dc power into microwave power, it inevitably also converts a significant portion of the dc power into heat. In many practical applications, only about half of the dc power is converted into microwave power; the other half is converted into heat. In fact, one can state that many state-of-the-art microwave power amplifiers are as much signal amplifier as they are electric heater; some of them are actually even more electrical heater than signal amplifier! The consequence of this is that the transistor may see a wide range of temperatures during the characterization measurements as well as during its operation.

As it happens, some of the electronic elements of the transistor are very sensitive to temperature. To illustrate what the consequences are on the transistor characterization process, let us revisit the simple BJT example described by (1) and (2). We once again apply a constant base current I_{B0} and a constant collector-emitter voltage V_{CE0} to a power transistor, and we take a look at the digital multimeters measuring the corresponding base-emitter voltage V_{BE} and the corresponding collector current I_C. If the transistor is biased in its active region, we will note that I_C slowly changes over time, to finally settle to a steady-state value. Note that such an effect, because of the time scale involved, cannot be explained by tiny inductors and capacitors since we are not applying any microwave frequency signal. The modeler may describe such a phenomenon by introducing the temperature (T) as an explicit parameter in the model equations (or in the equivalent circuit, which we consider as just another way to represent the model equations). The fact that the values of V_{BE} and I_C change versus time can then easily be explained by the fact that the temperature of the transistor starts changing due to self-heating as soon as we start our experiment. This can be expressed as

$$V_{BE}(t) = F_{BE}(V_{CE}, I_B, T(t)) , \tag{19}$$

$$I_C(t) = F_C(V_{CE}, I_B, T(t)) . \tag{20}$$

It is clear that a model can only be useful if it can accurately describe the effect of the time-varying temperature. To do so, the modeler needs to introduce concepts from thermodynamics, like thermal conductance (G_{th}) and heat capacity (C_{th}). To illustrate this fact, let us perform an approximate calculation of $T(t)$.

At the beginning of our experiment, the transistor temperature will be equal to the room temperature T_0. It will then start to rise because of the power dissipated in the transistor. In order to model the time-varying temperature, we need to write down the thermodynamic equations of our system. We further assume that our system can be represented by a heat capacity C_{th} and a thermal conductance G_{th}. The thermodynamic equation of our system becomes

$$\frac{d(C_{th}T(t))}{dt} = P(t) - G_{th}(T(t) - T_0) . \tag{21}$$

This classic equation simply expresses that, at any moment, the power dissipated in the transistor (P) minus the power that is conducted out of the transistor by the conduction of heat (proportional to the temperature difference with the environment $T - T_0$ and proportional to the thermal conductance G_{th}) is equal to the rate of change of the total heat stored in the transistor ($C_{th}T$). The introduction of the thermodynamic equations has direct consequences for the power transistor characterization. Let us solve the combined set of (20) and (21) to calculate $I_C(t)$. For the sake of simplicity, we will start by linearizing (20). We also approximate the dissipated power P by the product of V_{CE} and I_C

$$P(t) = V_{CE}I_C(t) . \tag{22}$$

The set of equations then becomes the following:

$$I_C(t) = F_C(V_{CE}, I_B, T_0) + \frac{\partial F_C}{\partial T}(T(t) - T_0) , \tag{23}$$

$$\frac{d(C_{th}T(t))}{dt} = V_{CE}I_C(t) - G_{th}(T(t) - T_0) . \tag{24}$$

The above "textbook" set of two coupled linear differential equations can easily be solved with as initial condition $T(0) = T_0$. The solution for the temperature $T(t)$ is given by a simple first-order relaxation, as shown below:

$$T(t) = T_0 + \Delta T_\infty(1 - e^{-t/\tau}) , \tag{25}$$

where ΔT_∞ is the steady-state temperature difference with room temperature and τ is the relaxation time constant. The values of these parameters are given below:

$$\Delta T_\infty = \frac{V_{CE}F_C(V_{CE}, I_B, T_0)}{G_{th} - V_{CE}\frac{\partial F_C}{\partial T}} \tag{26}$$

and

$$\tau = \frac{C_{th}}{G_{th} - V_{CE}\frac{\partial F_C}{\partial T}} . \tag{27}$$

The solution for the collector current is similar:

$$I_C(t) = F_C(V_{CE}, I_B, T_0) + \Delta I_\infty (1 - e^{-t/\tau}) , \qquad (28)$$

with

$$\Delta I_\infty = \frac{\partial F_C}{\partial T} \Delta T_\infty . \qquad (29)$$

The above results reveal an interesting property of the coupled electrical and thermodynamic equations (the so-called electro-thermal equations). From (26) and (27), we can conclude that the transistor, from the thermal point of view, behaves as a system with a heat capacity that is equal to C_{th}, but which has an apparent thermal conductance that is equal to the difference between the actual thermal conductance G_{th} and the product of V_{CE} and the partial derivative of $F_c(.)$ versus temperature T. We can conclude that if there is significant power dissipation in the transistor, we always observe a combination of thermal and electrical effects.

This can lead to interesting behavior. Suppose that we characterize a germanium bipolar transistor. Such transistors have a current gain that increases with temperature. The hotter the device, the more gain it has. This is mathematically expressed by

$$\frac{\partial F_C}{\partial T} > 0 . \qquad (30)$$

Consider now the right-hand side of (27). For some biasing conditions, especially at a high V_{CE}, the denominator can become negative. This occurs when

$$V_{CE} \frac{\partial F_C}{\partial T} > G_{th} . \qquad (31)$$

Under those conditions, we see that the relaxation time constant also becomes a negative number. And that means trouble! Putting the negative τ in (25) and (28), we come to the conclusion that the current as well as the temperature will exponentially increase, never to reach a steady-state value. This unstable positive feedback phenomenon is called "thermal runaway." The term is not only used in electronic engineering but also in chemical engineering, where it is more commonly known as a "big explosion." Fortunately for electronic engineers, the consequences of a thermal runaway are less severe and usually only result in a damaged transistor (a little bit of smoke may still be generated). Okay, so we have blown up one transistor and we go get another one. But how are we going to characterize the new device without also blowing it up? One way of breaking up the positive electro-thermal feedback cycle is to introduce a big enough resistor in series with the V_{CE} voltage source. The idea is that any increase in collector current will automatically decrease the collector voltage, decreasing the dissipated power, which then decreases the rate at which the temperature rises. This way we can characterize the transistor across its entire operating span without blowing it up. From the above example, we can conclude that it is hard to build one measurement setup that allows you to characterize all possible transistor technologies. One can imagine, for example, that an engineer is using the potentially unstable measurement setup during many years without blowing up any device due to thermal runaway simply because he is never measuring germanium transistors. One day, his manager gives him the task of characterizing a germanium transistor and, lo and behold, the "reliable" measurement system fails over and over again. Unless the engineer knows about thermal runaway, he will have a hard time facing his manager.

Consider now a microwave power transistor. If we apply a particular bias, the temperature of the transistor will slowly change with a relaxation time constant that can be anywhere from 200 ns to 1 ms, or even longer. At the same time, we can apply a microwave signal. If we look at a particular performance parameter of the transistor, like S-parameters or power gain, we will see that these parameters will also slowly drift as the amplifier moves to a new equilibrium temperature. Such an effect is called a "long-term memory" effect. In contrast, the dynamic effects caused by the inductors and capacitors described are sometimes called "short-term memory" effects. The precise characterization and modeling of the long-term memory effects is actually one of the toughest challenges faced by today's power transistor experts.

It is important at this point to state that long-term effects are not exclusively caused by a time-varying temperature. Other physical effects inside the transistor, called trapping effects, can cause similar behavior. The trapping effect is a long-term memory effect related to the fact that the charge distribution in an FET is influenced by charges that somehow get stuck in a trap and are only released after a relatively long time. These traps typically occur on the surface of the transistor, although they can sometimes also be found in the bulk. The amount of trapped charge is not a constant but depends on the region where the transistor operates. Since the operating region may vary significantly during transistor operation, the trapping state will also vary, but only at a slow rate that depends on how long it takes for the charge to be released by the trap after it has been captured.

Another important remark concerns the heat transfer (24). Equation (24) assumes that the thermal state of the transistor can be described by one temperature $T(t)$. If we have a big power transistor, one can imagine that the temperature is not constant across the transistor, but is a function of the location. In other words, the temperature is described as a scalar field rather than one particular number. It is perfectly possible, for example, that there are significant temperature differences between the fingers of the power transistor. In that case, the simple first-order model of (24) will not be sufficient

to describe the thermal behavior of the transistor. Note that it is not only the temperature that may vary inside the transistor, but that the same holds for the dissipated power. From the modeling point of view, such a case is usually resolved by connecting a multitude of thermal networks.

Why Pulsed Measurements Provide Answers

So how can we provide data to the modeler that allows him or her to model the long-term memory effects? If we are dealing with thermal issues, the simplest way would be to directly measure the temperature-dependent voltage-current relationship, as illustrated below for a bipolar transistor

$$V_{BE} = F_{BE}(V_{CE}, I_B, T)\,, \tag{32}$$

$$I_C = F_C(V_{CE}, I_B, T)\,. \tag{33}$$

This can only be done in practice if we apply a particular couple of values $\{V_{CE}, I_B\}$ for bipolar transistors or $\{V_{GS}, V_{DS}\}$ for FETs and a temperature T, and we make sure that we measure $\{V_{BE}, I_C\}$—or respectively $\{I_{GS}, I_{DS}\}$—before the temperature has significantly changed. Such a measurement is referred to as "isothermal." From the hardware perspective, this implies that we need to have means to control the temperature of the transistor, like a thermal chuck, such that it has a temperature T when we start the experiment, and that we need to be able to apply $\{V_{CE}, I_B\}$ or $\{V_{GS}, V_{DS}\}$ and make a quick measurement of $\{V_{BE}, I_C\}$ or $\{I_{GS}, I_{DS}\}$ before there is any significant change of the device temperature. Since we want to do more than one measurement, we switch $\{V_{CE}, I_B\}$ or $\{V_{GS}, V_{DS}\}$ off as quickly as possible after the experiment. We then wait until we are sure that the temperature has returned back to T before performing a subsequent measurement. If we can do all of this before there has been a significant change in temperature, we are able to directly measure the temperature-dependent $\{V_{BE}, I_C\}$ or $\{I_{GS}, I_{DS}\}$. This process is called pulsed bias or pulsed IV (PIV) characterization.

Note that there are many ways to perform pulsed measurements. In general, a lot of insight into the trapping behavior as well as the thermal behavior can be gained by not only changing the bias values during the pulse, but by also changing the initial bias values.

The technique of PIV characterization was pioneered in the late 1980s and further developed during the 1990s [4]–[9]. Figure 1 shows the result of a practical measurement performed on a 10-W GaN FET. The blue lines indicate the dc measurements, and the red and green lines represent two pulsed measurements, where each one has a different initial bias condition. One can clearly see that the IV relationship is a strong function of the initial conditions, and that the characteristics are very different from the dc measurements. Note that the dc measurements have been performed over a much smaller bias region than the pulsed measurements. This is typically the case since dc measurements stress the device much more than pulsed measurements. Pulsed measurements can easily be performed in regions where dc measurements would cause permanent damage to the device because of, for example, excessive heating.

As we stated before, a microwave amplifier cannot only be described by a set of static voltage/current

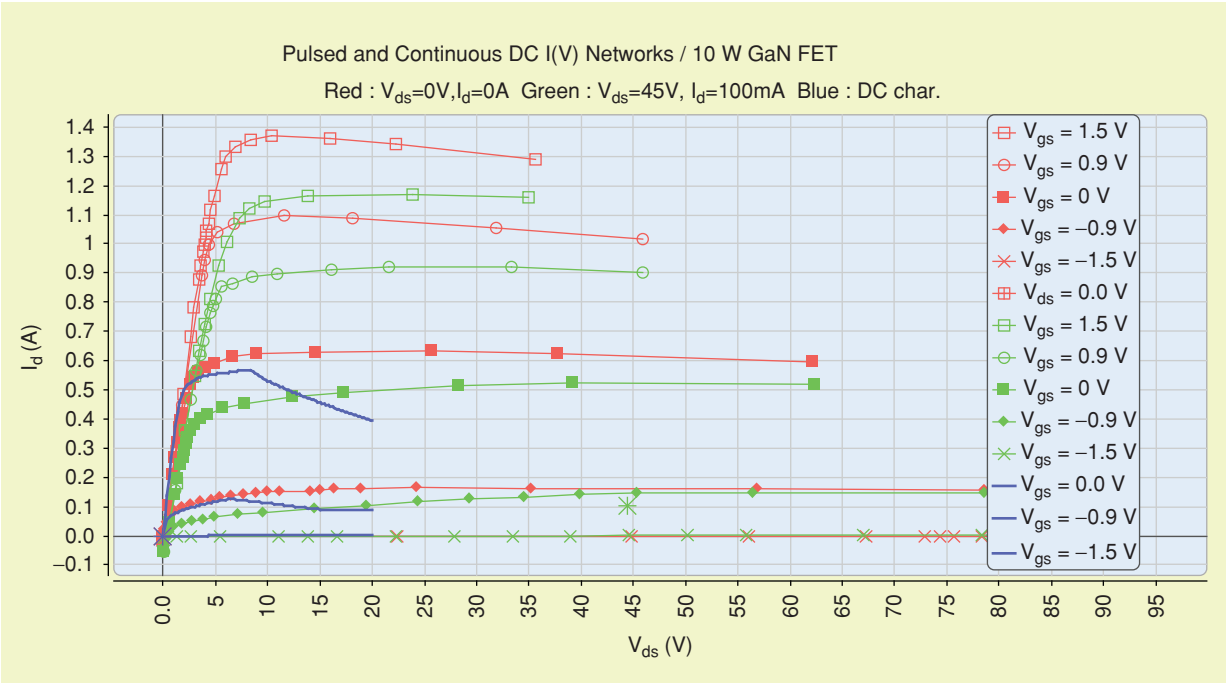

Figure 1. *Pulsed and continuous bias measurement example (red and green characteristics are pulsed, starting from different initial conditions).*

relationships. The model will also contain capacitive and inductive effects that need to be characterized. And, unfortunately, these are also a function of temperature. The idea is then to also measure the bias-dependent *S*-parameters under well-controlled isothermal conditions. Such measurements are called isothermal pulsed-bias *S*-parameter measurements. Adding *S*-parameter capability to PIV measurements was pioneered in the early 1990s [10], [11], and is still a hot topic today [12], [13]. A lot of excellent information on the above topics can be found in [14]. A practical example of pulsed-bias *S*-parameter measurements of a 20-W FET is shown in Figure 2.

Why Pulsed-Bias *S*-parameter Are Never Easy

Although the basic principle of pulsed-bias *S*-parameter measurements is relatively simple, it is actually a real challenge to carry them out in practice. Consider, for example, a practical self-heating phenomenon within an FET as presented in Figure 3. The figure is derived from a simulation and shows the temperature versus

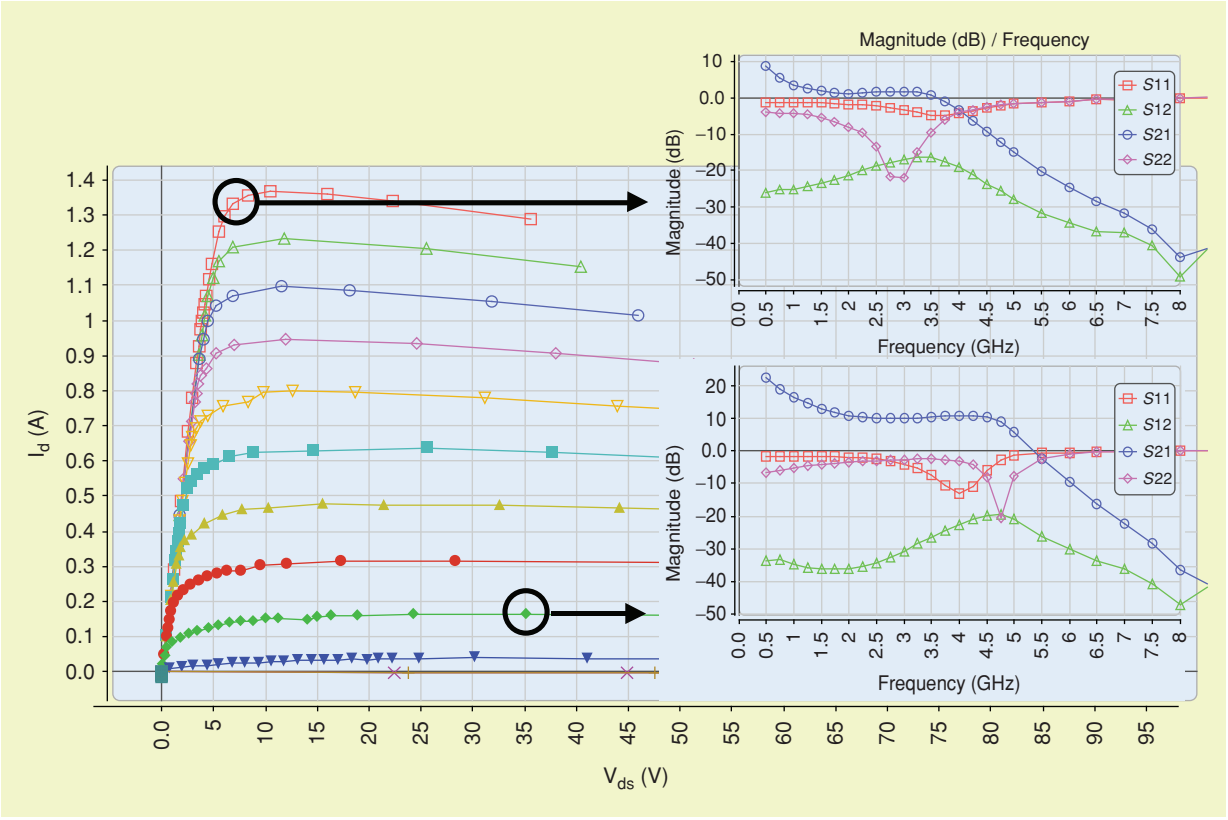

Figure 2. *Pulsed-bias S-parameter measurement example.*

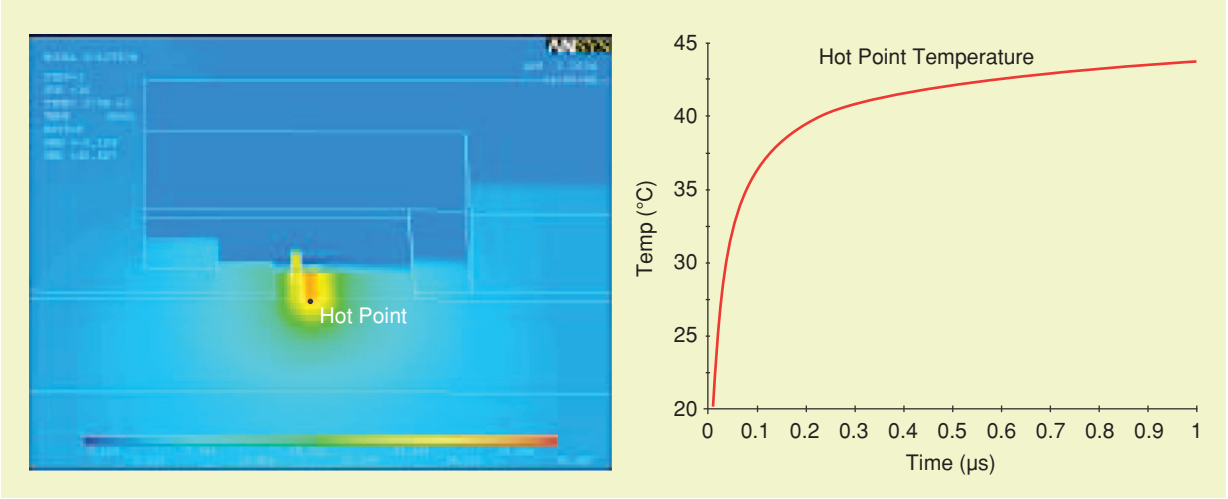

Figure 3. *Temperature increase of AlGaN/GaN HEMTs (SiC substrate), with a chuck temperature of 0°C.*

time when one applies an IV pulse to a transistor posed on a thermal chuck set at 0°C. In this example, the transistor gate measures 8 × 100 μm, and the pitch between the different fingers is 35 μm (SiC substrate). For an injected power of 5 W/mm, a thermal simulation using Ansys software shows a temperature increase of 41.5°C during the first 400 ns of the pulse. The temperature is calculated for a finger located in the middle of the transistor (the location of the temperature measurement is indicated by a point on the left). This simulation example shows that the transistor is not tested in isothermal conditions when applying IV pulse with a duration longer than about 400 ns. This implies that, in order to provide isothermal data to the modeler, we need to be able to measure the pulsed-bias *S*-parameters within a time span smaller than 400 ns. There are three main challenges to performing such a measurement, especially for new technologies such as GaN transistors.

First of all there is the challenge of generating and measuring the fast bias excitation pulses, which need transition times that are only a fraction of the pulse width, let's say 30 ns. Using recent metal-oxide semiconductor field-effect transistor (MOSFET) technologies, existing pulsers can deliver pulses up to 240 V or 20 A with an output resistance as low as 0.6 Ω. Figure 4 shows a typical voltage pulse shape obtained with a 200-MHz pulser delivering 100 V to a capacitance of 100 pF. These new high-power MOSFET technologies, with short switching times, offer new and exciting measurement capabilities for electro-thermal transistor modeling activities. When performing such measurements, one has to be very cautious about the presence of parasitic inductive and capacitive elements. Because of the steep slopes of the voltage and the current pulses, parasitic inductive and capacitive elements can easily cause ringing effects in the applied pulses as well as in the measured results. Parasitic small resistances can also distort the measurements. In fact, one needs a really careful design of the cabling between the pulses and the transistors. In general, one always tries to minimize the cable lengths as much as possible and tries to place the pulsed-bias generators as close as possible to the transistor terminals. Even then, it is a wise thing to characterize the parasitic behavior of your cabling and to correct any errors caused by parasitics of the measurement setup.

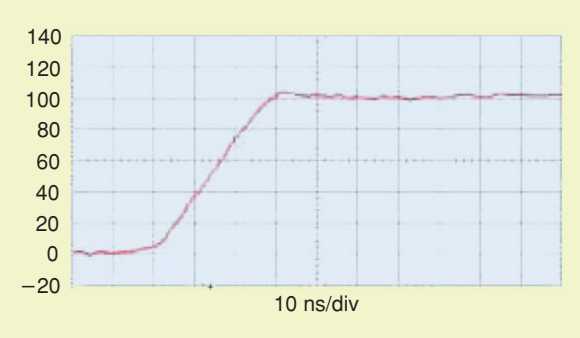

Figure 4. *Example of 100-V pulse voltage measurement using the latest pulser technology.*

Another issue is related to reliability. A complete characterization of a transistor requires the application of extreme pulsed-bias conditions, for example near the transistor breakdown area. Under such conditions, and when using a pulsed voltage generator, sudden breakdown effects may generate a spectacularly big current spike through the transistor. This current spike zaps the transistor and can even reduce the transistor to nothing more than a black spot on the wafer. To prevent this from happening, one can introduce a serial resistance between the transistor and the pulser. The resistance will then provide a robust and automated protection for breakdown current spikes. Besides providing protection, such resistive networks have other functionalities. A high input serial resistance associated with a pulsed voltage generator behaves like a current source and can be used to drive a bipolar transistor whereby one has accurate control of the pulsed input base current. This is especially interesting when the temperature of the transistor changes and modifies the base-emitter diode characteristic. In addition, the resistive network can also be adjusted to lower the risk of low-frequency parametric oscillations. An example of a pulsed-bias setup with a resistive network is shown in Figure 5.

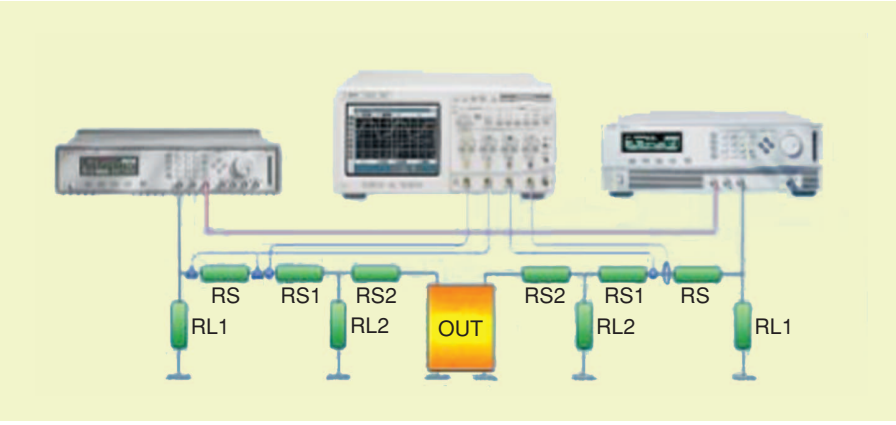

Figure 5. *Pulsed-bias measurement system with resistive network.*

All of the effects mentioned above have to do with the problem of performing pulsed-bias measurements. But the *S*-parameter measurements are also challenging because they need to be made under pulsed conditions. Between the early 1990s and 2000s, the HP-8510 vector network analyzer (VNA) was a popular tool for making pulsed *S*-parameter measurements. The

instrument could make *S*-parameter measurements with a good dynamic range for all pulses having duration of more than 1 μs. Unfortunately, as explained previously, such a pulse width is too long for the isothermal characterization of certain modern power transistors. Using a different operating mode, called narrowband mode or asynchronous mode, VNAs could measure RF pulses as short as 150 ns, but not without a severe desensitization that was proportional to the duty cycle. This could be resolved by averaging, but at the cost of significantly decreasing the measurement speed. Today, improved ways of measuring pulsed scattering parameters have become readily available with the advent of a new generation of VNAs. In addition to having better hardware, the dynamic range of pulsed measurements is further improved by using techniques like hardware and software algorithms [12]. It is now possible to make pulsed *S*-parameter measurements in the *X*-band with a dynamic range better than 50 dB using a pulse width of 150 ns and a duty cycle of 0.001%.

Validating Models with Load-Pull Measurements

Isothermal pulsed-bias *S*-parameter measurements allow the modeler to construct an equivalent electrical network, called the transistor model. This model can represent the transistor in a simulator. If the modeler has done a good job, the equivalent electrical network that he or she has built will behave in a way that is consistent with the measured data. In other words, if one were to simulate the isothermal pulsed-bias *S*-parameter measurements, the simulated response of the device would closely match the actual measured data. At that point, the modeler can send the model to the designer. One can then imagine the following conversation taking place:

> Designer: "How can you be so sure that your model will correctly predict the transistor behavior for my amplifier design project?"
>
> Modeler: "Well, if you would use that model to simulate isothermal pulsed-bias *S*-parameter measurements, the simulated data will precisely match the measured data."
>
> Designer: "I believe you. But I am not interested in simulating isothermal pulsed-bias *S*-parameter measurements. I need to simulate under real operating conditions, with real signals. So I repeat my question: How can you be so sure that your model will correctly predict the transistor behavior for my amplifier design project?"
>
> Modeler: "Well, I pretty much used the same kind of equivalent circuit that worked before. To make it match the measured pulsed-bias *S*-parameter data, I only had to add a tiny nonlinear capacitor to the circuit and I had to introduce one new parameter to the mathematical function that describes the nonlinear current source."
>
> Designer: "You actually had to add new things to the existing model to match your data??? Now I am really worried. I won't start using your model unless you show me that it also works under realistic operating conditions!"

The idea is that a designer will simply not trust a model derived from pulsed-bias *S*-parameter measurements unless the model has been experimentally characterized under realistic operating conditions. This leads us to a different branch of microwave power transistor characterization where the goal is to validate a model and not to extract the parameters of the model. Model validation is done by stimulating a transistor with excitation signals that are very similar to the actual signals the device will experience in a power amplifier and by measuring certain characteristics that can be derived from the response signals, such as power gain and spectral regrowth. The designer will start trusting a model only when it is capable of accurately predicting the derived quantities of interest to the designer, and over a range of excitation signals that matches the final application.

So what do validation systems look like? Refering to the example conversation between the designer and the modeler, it is clear that the most significant difference with the pulsed-bias *S*-parameter system will be the power of the applied microwave signals. The validation system needs to apply microwave signals that, by themselves, are able to sweep across the whole transistor operating region, whereas a pulsed-bias *S*-parameter system will only use relatively small microwave signals and will cover the transistor operating region by means of pulsing the bias. But power is not the only parameter; there are other, more subtle, differences. At microwave frequencies, a pulsed-bias *S*-parameter system will always terminate the transistor terminals into a 50-Ω load. In microwave power amplifiers, the transistor output is terminated in a wide range of impedances that spans anywhere from about 1 Ω to about 200 Ω. This implies that a validation system needs to provide three main functions: exciting the transistor with sufficient microwave power, controlling the output impedance, and measuring the response signal of the transistor. Controlling the output impedance is often referred to as "load-pull," which is why systems that have this capability are called load-pull systems. In the following, we give an overview of existing load-pull techniques. Note that one sometimes also controls the output impedance of the signal generator. This is called "source-pull."

As described in [15], load-pull systems are typically classified into two main categories: active and passive.

In a passive load-pull system, the load impedance is controlled by passive tuners. The passive tuner is usually mechanical in nature, whereby a metal part is moving in a waveguide in order to create controllable reflections. A good example is described in [16]. A small fraction of passive load-pull setups are actually electronic in nature and use diodes to generate a multitude of reflection coefficients, as described in [17].

The major drawback of using a passive structure to create a controllable reflection is that one cannot compensate for any power that is dissipated between the device under test (DUT) and the passive structure that generates the controllable reflection. This power dissipation inevitably occurs in all components that are placed between the transistor terminal and the tuning elements such as probes, cables, couplers, diplexers, etc. As a result, the maximum amplitude of the reflection coefficient, as seen by the transistor, will always be smaller than one. Depending on the amount of inevitable losses in the measurement setup, the maximum amplitude of the reflection coefficient may become too small to be of any use. This problem may be solved by using so-called active load-pull setups. These are setups in which one introduces one or more amplifiers to generate wave signals that are sent towards the DUT output terminals. The amplifier can potentially compensate for any losses and generate reflection coefficients with amplitudes equal to and even bigger than one.

A good example, illustrating the problems and benefits of active load-pull, is described in [18]. Unfortunately, there are not only advantages to using an active load-pull approach. The power handling capability of any active load-pull setup is limited by the amplifier that is used. This limits both the maximum power handling capability as well as the frequency range over which one can synthesize impedances. In contrast to the active load-pull setups, the maximum power handling capability and frequency range of any passive load-pull setup is only limited by passive structures like cables, couplers, etc. Passive tuners typically operate across multiple octaves and can handle power levels above 1 kW. Today, the vast majority of the load-pull setups use passive mechanical tuners. It is worth noting that the typical mismatch of a GaN transistor is relatively mild and within reach of most simple mechanical tuners, in contrast with silicon laterally diffused metal oxide semiconductor (LDMOS) transistors which have output impedances below 1 Ω.

An example of an advanced classic load-pull setup is depicted in Figure 6. A load and a source tuner are placed as close as possible to the DUT, a power transistor. The two tuners provide a whole range of possible input and output impedances. The input signal is provided by a synthesizer, often boosted by a power amplifier. A VNA and a power meter are used to measure the RF signals. A bias supply and monitoring system are also present. The setup can stimulate the transistor with a realistic, high-power microwave signal while at the same time presenting a realistic output impedance. It is not that trivial, however, to determine actual performance parameters of the transistor, such as output power, power gain, or power-added-efficiency (PAE). The main reason is that our power reading is taken after the tuner and not at the transistor output terminal. The transistor performance can only be calculated by using a combination of the power meter reading with the VNA measurements, the measured bias voltages and currents, and, finally, the *S*-parameters of the tuners. Note that these *S*-parameters are a function of the tuner settings; they are different for each realized input or output impedance. These *S*-parameter functions are determined a priori by a time-consuming tuner calibration procedure whereby one measures the *S*-parameters for a whole range of tuner settings, usually covering the whole Smith chart.

There exist many variations of the load-pull system depicted in Figure 6. For example, some systems are simpler because they do not have the input coupler and VNA. Some systems are more complex—for example, using a spectrum analyzer instead of a power meter. Of course, the simpler systems provide less information on the transistor behavior than the more complex ones. If one eliminates the input coupler and VNA, for example, it is impossible to determine the power absorbed at the input of the transistor. This implies that, using such a simplified system, one can only measure the output power generated by the transistor, but that one cannot determine other parameters like power gain or PAE. Adding a spectrum analyzer, on the other hand, allows you to measure the amplitude of the harmonics or the amount of spectral regrowth—information that one simply cannot get with a simple power sensor measurement.

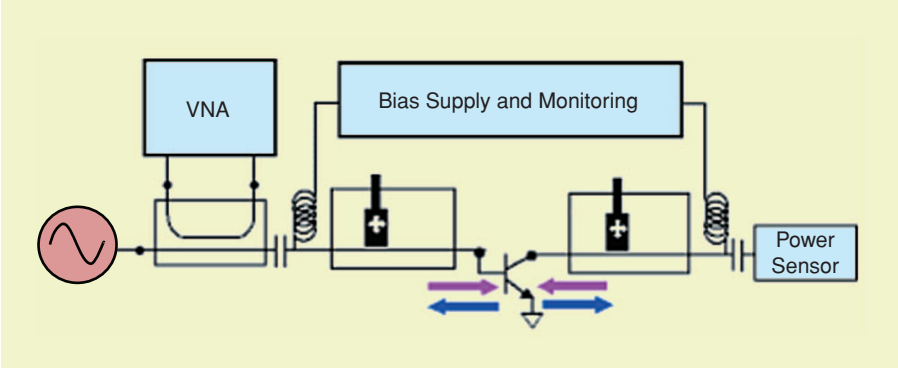

Figure 6. *Schematic of a classic load-pull setup.*

Most load-pull systems control the load impedance and perform power measurements only at the frequency of the input signal, the so-called fundamental frequency. Any large-signal excitation of the power transistor will not only generate output power at the fundamental frequency, but also at multiples of the fundamental frequency. These spectral components are called harmonics. As there is power in the harmonics, the overall behavior of the transistor will not only depend on the load impedance at the fundamental frequency but also on the load impedances at the harmonic frequencies. Some load-pull systems control the load impedance at the second and even the third harmonic frequency [16], [19], [20]. Such systems are called harmonic load-pull systems.

Load-Pull and Time Domain

Classic load-pull systems allow one to verify whether a model can accurately predict power levels under load-pull operating conditions. Unfortunately, power is not the only parameter that is of interest. The modeler also needs to validate the capability of his or her model to describe other important aspects, such as breakdown effects or forward gate conductance. A validation of the model for such highly nonlinear effects can only be achieved by actually measuring the time-domain voltage and current waveforms under realistic large-signal operating conditions and comparing them with the time-domain waveforms that result from a simulation.

Load-pull systems having the capability to provide such time-domain voltage and current waveforms were first developed in the late 1990s [24], [25] by adding tuning technology to large-signal network analyzers [26]. Large-signal network analyzer technology itself was developed during the late 1980s and the 1990s [21]–[23]. Note that all of the power information that is measured by a classical load-pull system can easily be derived from the time-domain voltage and current waveforms.

Figure 7 represents a typical schematic of a modern time-domain load-pull system. The incident voltage wave signals are represented by A_1 and A_2, and the scattered voltage wave signals are represented by B_1 and B_2. The subscript in the notation refers to the respective test port. The voltage waves A_1, B_1, A_2, and B_2 are sensed between the tuner and the transistor terminal by a dual directional coupling structure and are measured in the time domain by a broadband receiver. The voltage wave signals A_1, B_1, A_2, and B_2 are then converted into voltage and current waveforms V_1, I_1, V_2, and I_2 [26].

At the heart of the time-domain load-pull system is the broadband receiver. The oldest approach is to use a mixer-based receiver [22]. Such a receiver is leveraged from existing VNAs and measures the fundamental and the harmonics one by one, aligning the phases of all harmonics by means of a reference channel that is excited by a multiharmonic reference signal. A modern version of the mixer-based time-domain receiver is described in [27]. An alternative solution is based on the use of a four-channel repetitive-sampling frequency convertor [28].

Note that in a time-domain load-pull system, one always puts the directional coupling structure between the transistor and the tuner. The advantage of this approach is that the measured voltage waves, just by themselves, completely determine the voltage waves at the transistor terminals, and it is not necessary to know the *S*-parameters of the tuner. In fact, the information on the impedances represented by the tuner can be derived from the measurements. As such, the time-domain load-pull setup no longer requires any a priori characterization of the tuners. A second advantage is that the setup can always sense all significant harmonics signals. This is not true with the classical load-pull configuration where the harmonic information is often blocked by the tuner and, as such, cannot be sensed after the tuner.

Unfortunately, putting the directional coupling structure between the transistor and the tuner may cause losses that result in a degradation of the range of impedances that the tuner can generate at the terminals of the transistor. This issue is addressed by using extremely low-loss directional coupling structures. Currently, there are basically two solutions: one can use a specialized distributed coupler design [29] or one can use a wave probe [30].

The wave probe is a loop coupler with a very tiny loop, the loop being significantly smaller than a quarter-wavelength of the highest frequency to be measured. The principle was published more than 60 years ago [31]–[34]. The loop introduces virtually no insertion loss, yet has a directivity that is sufficient for all load-pull applications.

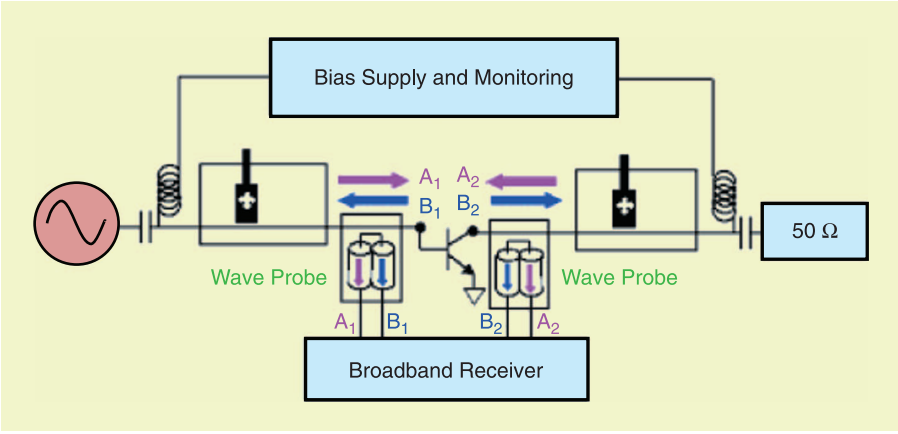

Figure 7. *Schematic of a time-domain load-pull setup.*

Figure 8 depicts a loop coupler that is positioned close to the center conductor of a waveguide structure. Note that the ground of the waveguide is not represented. Assume that a traveling voltage wave (denoted by *A*) is traveling from right to left inside the waveguide. The electric field caused by the charge on the center conductor induces a current in the left arm of the wave probe that is in phase with the current induced in the right arm. The magnetic field, on the other hand, induces two currents in both arms of the wave probe that are in opposite phase. If the loop is dimensioned such that it has the same amount of electric and magnetic coupling, there is destructive interference between the electrically and magnetically induced currents in the left arm, whereas there is constructive interference in the right arm. Thus, a signal is only generated in the right arm and not in the left arm of the wave probe, thereby demonstrating the directivity of the structure. The coupling effect of a wave probe is effectively localized, in contrast to classical distributed couplers.

Probably the most important characteristic of the wave probe is its directivity. The directivity of a coupling structure is the quantitative measure of its ability to separate the two waves traveling in the transmission line structure. In Figure 8, for example, the directivity is given by the ratio between the power measured at the right output of the wave probe and the power measured at the left output of the wave probe, under the assumption that there is only a wave traveling to the right on the main structure (as it is the case in Figure 8). A simple wave probe has a directivity of about 12 dB, which is sufficient for load-pull applications. Another important characteristic of the coupling structure is the coupling factor versus frequency. Figure 9 depicts the coupling factor versus a wide band of frequencies, for different distances between the wave probe and the center conductor of a transmission line structure. These measurement results show a coupling factor that increases with frequency, until about 10 GHz. The coupling factors range from about −20 dB to −40 dB. The increase of the coupling factor for higher frequencies can be beneficial for harmonic measurements. This can be explained by the fact that losses in cables and connectors increase with frequency and by the fact that power levels of harmonics are lower than the power level of the fundamental. The wave probe can automatically boost the power of the higher-frequency harmonics relative to the power of the lower-frequency fundamental. This power-leveling effect increases the dynamic range for the harmonics. In our example, we use a coupling factor of the wave probe between −50 dB and −40 dB in the *S*-band [2–4 GHz]. The outputs of the wave probe are directly connected to RF samplers that can handle a maximal input power of about −10 dBm. As such, the setup used for the example can handle power levels up to 40 dBm. We can control the distance between the wave probe and the center conductor of

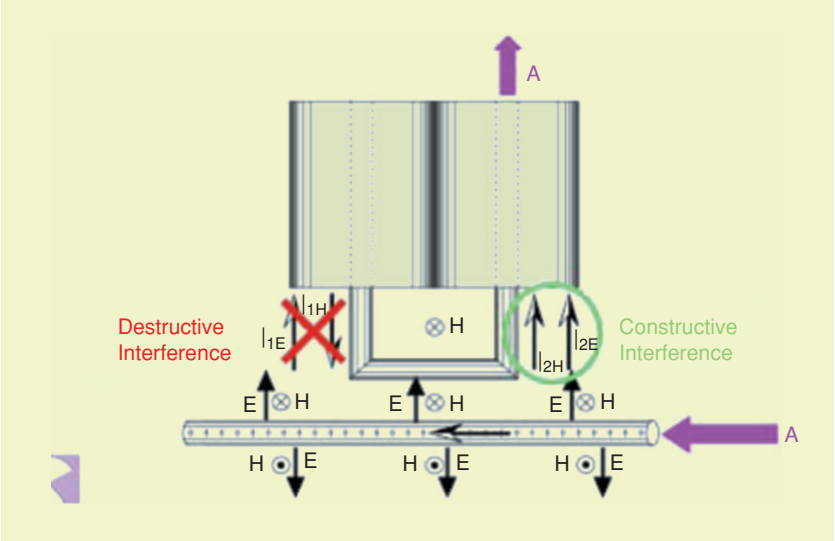

Figure 8. *Loop coupler structure inserted near the center conductor of a transverse electromagnetic mode (TEM) waveguide structure.*

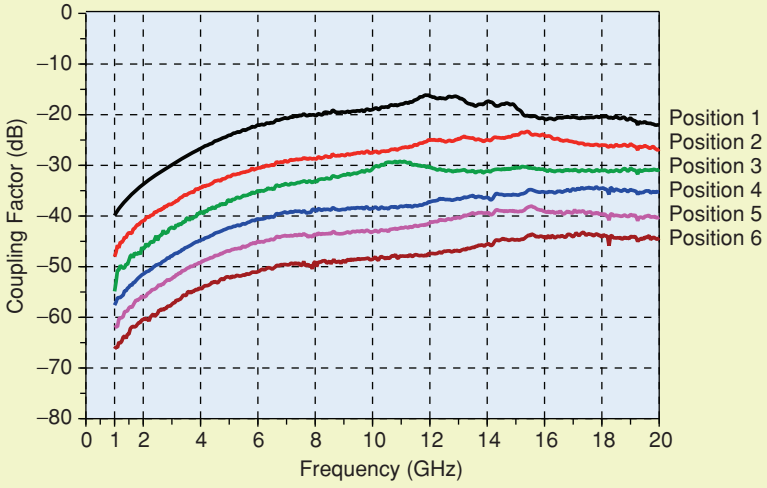

Figure 9. *Coupling value of a wave probe for different positions above the main line in the band (1–20 GHz).*

the transmission line, which enables one to optimize the setup for a specific power level.

Figure 10 shows a picture of the time-domain load-pull system with wave probes at XLIM/University of Limoges (France). Figures 11 and 12 show examples of time-domain load-pull measurements that have been performed on the system. Figure 11 shows the drain voltage and drain current waveforms at the terminals of a GaN high electron mobility transistor (HEMT), corresponding to a power sweep at 2 GHz. Note the highly nonlinear effects in the waveforms that cannot be characterized by classic load-pull techniques. Figure 12 shows the corresponding dynamic load line representation of voltage and current waveform measurements. The device was measured under the following operating conditions: $F_0 = 2$ GHz with seven harmonic frequencies measured, $V_{ds} = 25$ V, $V_{gs} = -5$ V, $I_{ds} = 7$ mA, $Z_{\text{load}} = (24 + j6)\ \Omega$. In a dynamic load line representation, one plots the drain current versus the drain voltage, which is a valuable tool for amplifier designers. Prior to the existence of time-domain load-pull systems, there was no way to measure these dynamic load lines and they were only useful in simulators.

Other Interesting and Future Developments

During the last decade, power transistors have needed to be characterized at ever-decreasing load impedances. Some high-power transistors, like LDMOS transistors for base station applications, need to be characterized at load impedances as low as 1 Ω. Unfortunately, tuner technology is constructed using 50-Ω transmission lines, having 50-Ω coaxial connectors. The significant difference between the impedances to be synthesized and the characteristic impedance of the tuner causes all kinds of problems like a deterioration of the tuning range (compared to the range of interest), as well as poorly conditioned measurements. A practical solution is offered by using tapered lines as impedance transforming networks. An example of such a structure is given in Figure 13. The figure shows a Klopfenstein 50-to-7.15-Ω transformer [35]. The impedance transformer shown is used to characterize a 100-W LDMOS transistor.

Another interesting development is the advent of power transistors that are contacted through a set of balanced terminals (differential terminals) rather than unbalanced terminals (signal-ground connection). It is very hard to perform load-pull measurements on such components because of the need to control the differential impedance, and often also the common-mode impedance. Two solutions have recently been developed. The first one is a passive differential tuner, as depicted in Figure 14. The tuner is constructed by carefully aligning and synchronizing two tuner sections into one mechanical structure [36]. An alternative solution is the differential active load-pull setup as described in detail in [37]. In this approach the differential and common-mode impedances are actively synthesized by carefully controlling the phase and amplitude of the injected waves at each of the differential terminals.

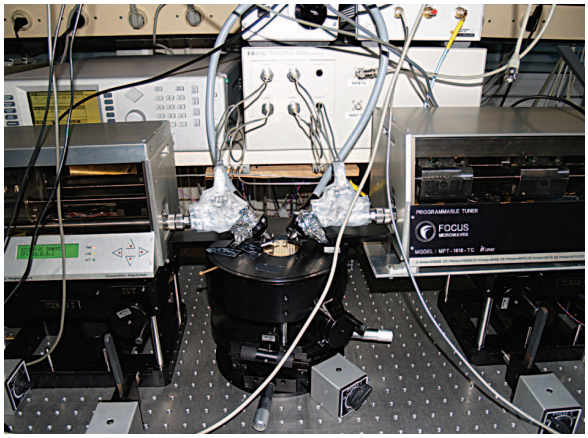

Figure 10. *Photograph of a time-domain load-pull system containing wave probes. (Photo courtesy of XLIM, France.)*

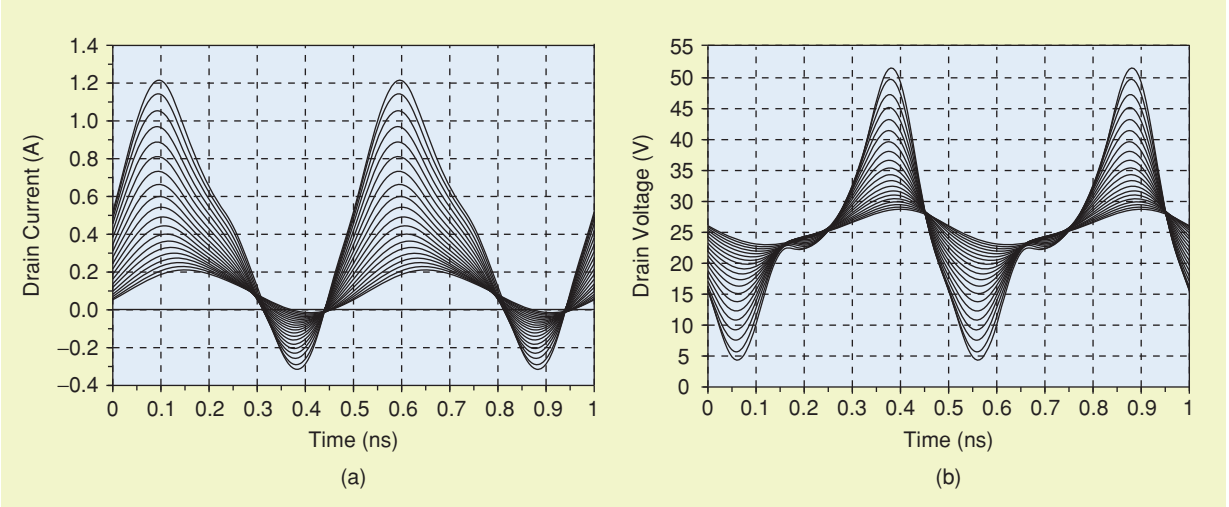

Figure 11. *Drain voltage and current waveforms measured by a time-domain load-pull system.*

As explained in this article, one can divide microwave power transistor characterization into two areas: model extraction measurements on the one hand and model validation measurements on the other. An interesting topic is the development of model extraction techniques that are directly based on large-signal measurements, which can actually be considered as a superset of *S*-parameter measurements [38]. Although this is an appealing idea, it turns out to be extremely difficult to apply in practice because it is hard to explore the whole operating region of the transistor by means of large-signal waveforms, in contrast to using a pulsed-bias technique. A combination of pulsed time-domain load-pull measurements that are synchronized to pulsed-bias measurements may be a promising approach to solve this issue.

Finally, an interesting development relates to the measurement of the time-varying temperature in transistors under large-signal operating conditions. Such measurements directly characterize the thermodynamic effects of microwave power transistors. One can use infrared thermal imaging [40] or more advanced fast optical interferometry [39].

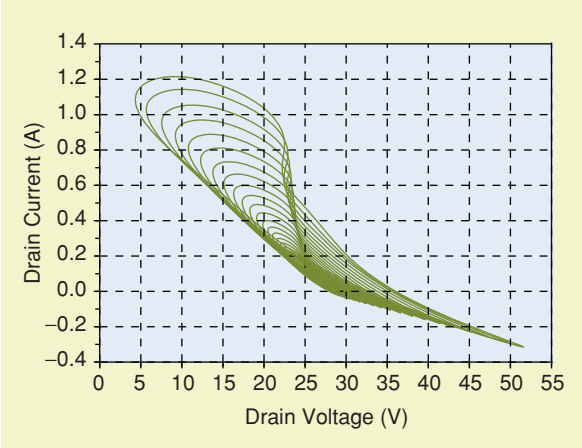

Figure 12. *Dynamic load line measured with a time-domain load-pull system.*

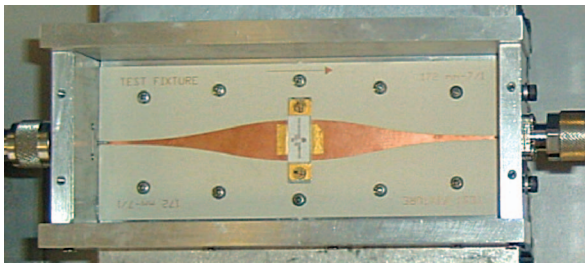

Figure 13. *Klopfenstein impedance transformer. (Photo courtesy of Prof. Paul Tasker, Cardiff University.)*

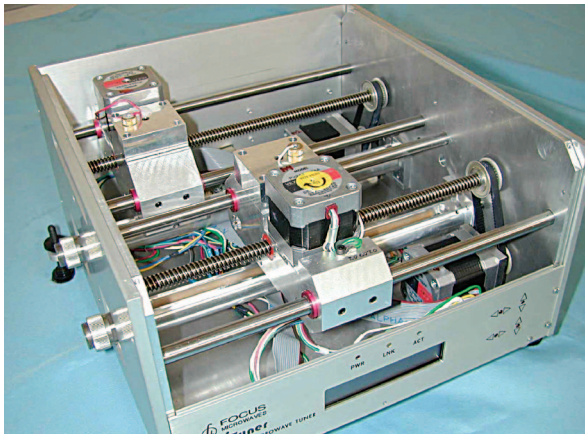

Figure 14. *Differential tuner. (Photo courtesy of Focus Microwaves.)*

The Whole Truth

We have considered microwave power transistor characterization exclusively as a tool that supports modelers, either for model extraction purposes or for model validation purposes. This can be considered as a modern way of thinking about the subject, especially when it concerns load-pull measurements. Load-pull measurements were actually in use long before the first large-signal microwave simulator saw the light of day. Experienced designers can succeed in building a good power amplifier without using any simulations at all [1]. Instead, they use the load-pull system as a kind of analog simulator. The idea is to experimentally determine the optimal matching conditions for the transistor in order to meet the amplifier requirements, rather than optimizing the design in a simulator. It is then sufficient to build the design such that it presents the same impedances as the optimal ones determined by the load-pull experiment.

Conclusions

The characterization of microwave power transistors is an important and emerging field with many interesting engineering challenges. One can basically distinguish two areas: model extraction measurements and model validation measurements.

To make things simple, isothermal pulsed-bias pulsed *S*-parameter measurements are typically used for model extraction purposes and load-pull measurements are typically used for model validation purposes. Both areas are rapidly evolving in order to keep track of new power transistor technology. The main issue with pulsed-bias pulsed *S*-parameter characterization is the need to apply pulses with ever-increasing amplitude (up to 200 V and 10 A) and ever-decreasing pulse width (smaller than 400 ns). The load-pull measurements can be done with a variety of setups, with active or passive approaches, and with or without handling harmonic frequencies. The challenges of load-pull system development are to offer time-domain voltage and current waveforms at the transistor terminals—an invaluable tool to provide insight in highly nonlinear transistor behavior—in addition to the capability to present low input impedances (1 Ω) and to handle high power levels (up to 100 W).

A new interesting topic is the development of model extraction techniques that are directly based on large-signal measurements [38]. A combination of pulsed time-domain load-pull measurements that are synchronized to pulsed-bias measurements may be a promising approach to solve this issue.

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