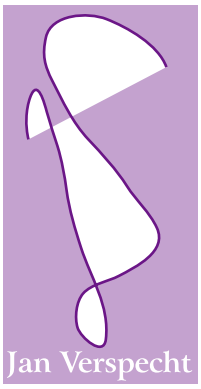

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High power on-wafer capabilities of a time domain load-pull setup

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***Abstract*— High power LSNA on-wafer measurements up to 20 Watts at 2 GHz have been performed on a 3.2 mm gate width AlGaN/GaN HEMT. Time domain slopes in pulsed mode are given for different pulsed drain voltages, showing the importance to monitor the drain voltage and current slopes, as they are directly linked to the transistor reliability. At such power range, the LSNA on-wafer load-pull setup with two 'wave probes' couplers demonstrates its capabilities to handle up-to-date power transistors in the S band, and to provide the time domain information usually missing with classical load-pull setups.**

***Index Terms* — LSNA, on-wafer measurements, power transistors, reliability, time domain measurements**

I. Introduction

The needs in the field of telecommunications in terms of transistor performances are strongly increasing, particularly for their output power and PAE. A classical objective is to obtain tenths of Watts in the L and S frequency bands [1] [2]. But a high output power induces high drain voltages and currents [3]. Thus it is of great interest for designers to look at maximum voltages and currents slopes for reliability issues. We have built with the LSNA a time domain pulsed load-pull setup operating at high power levels.

High power on-wafer measurements are presented here, up to 20 Watts (6.3 W/mm) at 2 GHz in pulsed mode with 8 harmonic frequencies taken into account. A comparison between time domain slopes for different drain bias voltages is shown, demonstrating the interest of time domain high power measurements for transistor reliability issues.

II. Setup and Transistor Descriptions

A kind of time domain load-pull setup has been described in [4] [5]. Classical couplers are replaced by the so-called 'wave probes'. Two wave probes are connected to a LSNA to capture at both DUT ports the incident and reflected waves. The two most important capabilities of this setup are:

- Measurement up to several tenths of watts in the S band;
- Pulsed capabilities for bias and RF measurements without any RF accuracy reduction due to the duty cycle.

The description of the setup is given on Fig. 1. Note that this kind of organization can handle on-wafer measurements [6] as well as more classical high power "connected" said ones.

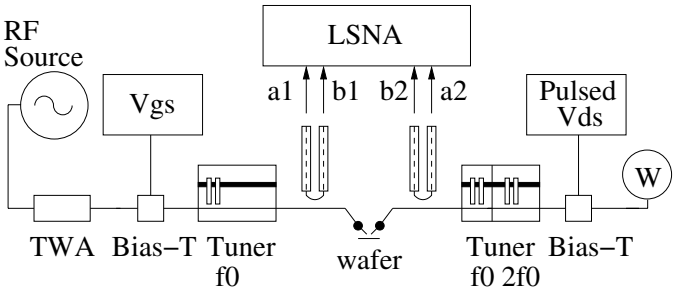

Fig. 1 Setup for time domain load-pull on-wafer characterizations

For all the following measurements, the transistor and measurement characteristics are:

- AlGaN/GaN HEMT, processed by Alcatel-Thalès III-V lab (France);
- Gate development: 3.2 mm (8x400 µm);
- F0 = 2 GHz
- measurements up to 8 harmonic frequencies;
- Gate voltage: continuous mode V_{GS} = -3.7 V
- Drain voltage: pulsed mode, bias V_{DS0} = 0 V;
- RF input power and drain biasing: pulsed mode 5 µs / 100 µs;
- Class B.

The considered duty cycle is 0.05. So the pulsed measurement technique described in [7] is performed to improve time domain measurements. As there is no dynamic range loss, even with this very small duty cycle, a maximum number of

harmonic frequencies can be measured, only limited by the setup (connectors, cables).

III. High Power Transistor Measurements

Fig. 2 gives the output power versus the input power for the following settings:

- Load impedance: (40+j.31) Ω;
- Pulse drain voltage: 67 V

This slope reaches an output power of 20.2 Watts, with a power gain of 14 dB and at a power gain compression limited to 4 dB. For the same input power sweep, Fig. 3 gives the PAE. At the maximum output power, the PAE is 48 %; it means a total power of near 43 W is handled by the wafer probes during the pulses. Thanks to the association of wave probes and the sampling receiver, the extrinsic load line is available even at this RF power range.

Fig. 4 shows the load lines for the highest part of the input power sweep. We can observe here that the transistor, with the load impedance mentioned above, runs close to 120 V and more than 1.6 Amps to reach 20.2 Watts at 2 GHz.

IV. Power versus Reliability

A good nonlinear transistor model is of great interest for the efficient design of high power amplifiers. But these models are usually at least inaccurate and sometimes completely wrong in the high power breakdown area, especially for pulsed applications. Even the most sophisticated pulsed I(V) and pulsed S-parameters measurements devoted to modeling cannot represent in a general manner and for any biasing / load / pulse configuration the behavior of large transistors. So, there is always a model uncertainty with the CAD design of high power amplifiers. A transistor measurement with real operating conditions is the only way to get confident about the model reliability and the device behavior, especially if the RF load lines are entering the breakdown area [8] [9] [10] [11].

Fig 5 gives different slopes of output power versus input power for several pulse drain voltages and load impedances:

- V_{DS} = 25 V with Z_{load} = (42+j.17) Ω
- V_{DS} = 40 V with Z_{load} = (42+j.17) Ω
- V_{DS} = 55 V with Z_{load} = (48+j.14) Ω
- V_{DS} = 67 V with Z_{load} = (40+j.31) Ω

As expected, the available output power at a given power gain compression is increasing with the pulsed drain bias voltage, and Fig. 6 gives the maximum output power versus the pulse drain voltage for a power gain compression of 4 dB and for the load impedances given above.

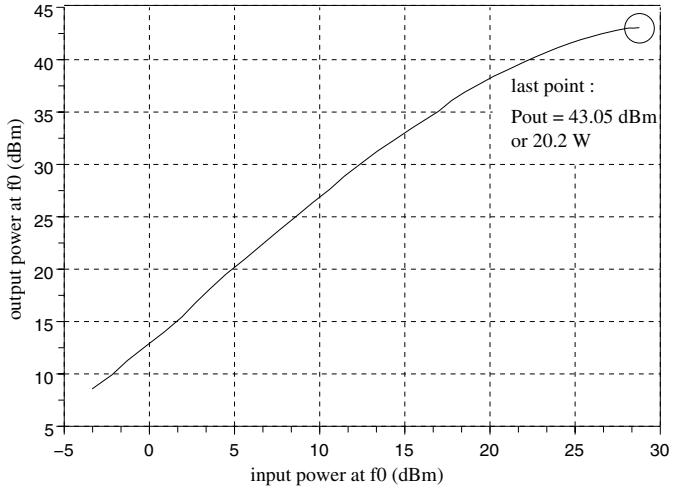

Fig. 2 Output power at f0 versus input power at f0 ; AlGaN/GaN HEMT, gate development: 3.2 mm, f0: 2 GHz, pulse drain voltage: 67 V, RF and drain voltage: 5µs/100µs, class B

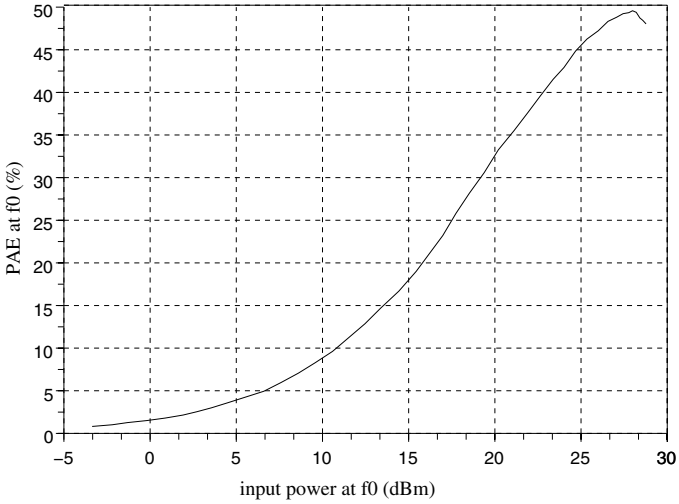

Fig. 3 PAE (%) in the same conditions described at Fig. 2

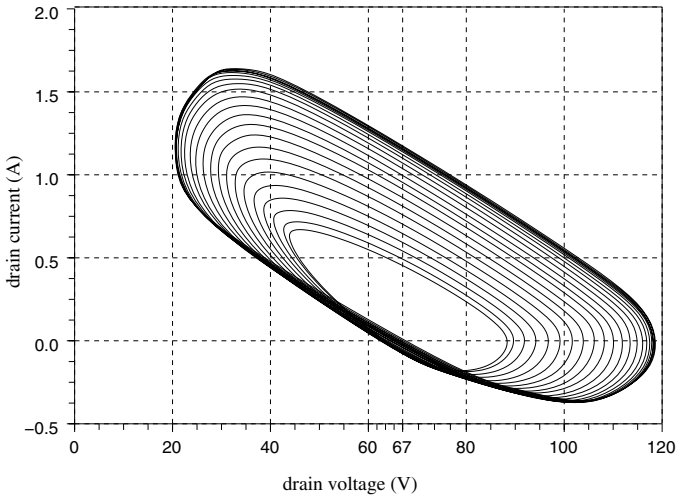

Fig. 4 Load lines corresponding to the same input power sweep of Fig. 2. Eight harmonic frequencies are measured.

Fig. 7 shows the extrinsic load line at a compression of 4 dB for all these four measurement conditions. If the designer knows that there is a limit in terms of voltage or current, he can compare them with the time domain measurement results to choose acceptable load impedance and output power.

V. Conclusions

Two capabilities of a time domain load-pull setup are pointed out: pulsed measurements and high power measurements with an example at 20 W / 2 GHz. This very high power range for on-wafer measurements is a key point for modern power amplifier conceptions. The reliability of these amplifiers can be improved by monitoring the drain IV maximum values.

Acknowledgment

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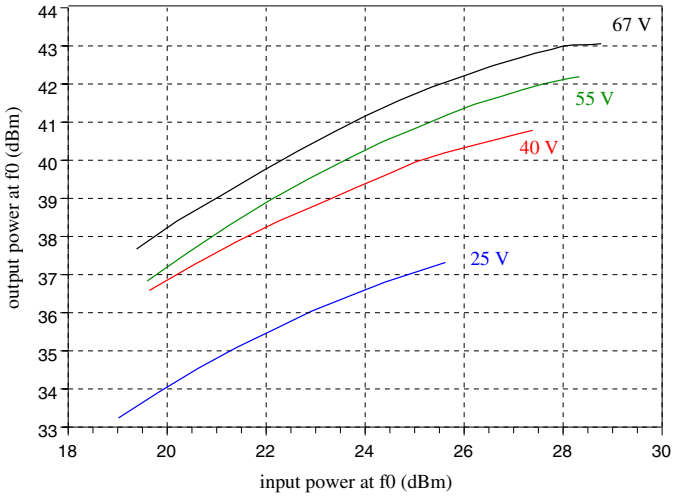

Fig. 5 Comparison of output power at f0 for different input power sweeps corresponding to different pulse drain voltages: 25V (blue), 40V (red), 55V (green) and 67V (black).

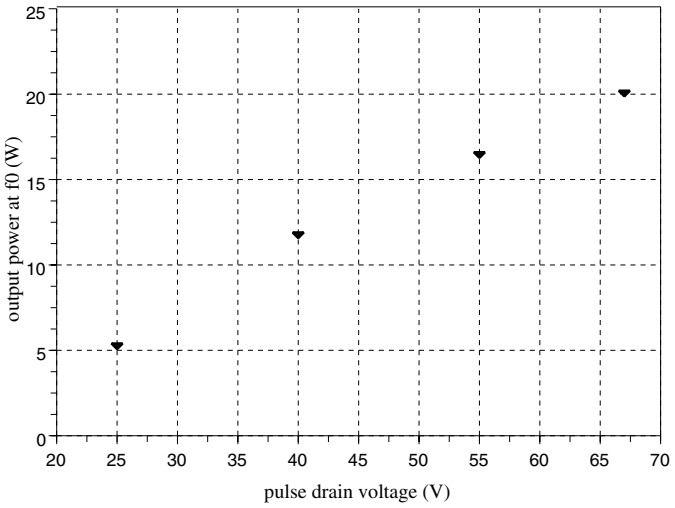

Fig. 6 "Maximum" output power at f0 for different pulse drain voltages; power gain compression: 4 dB

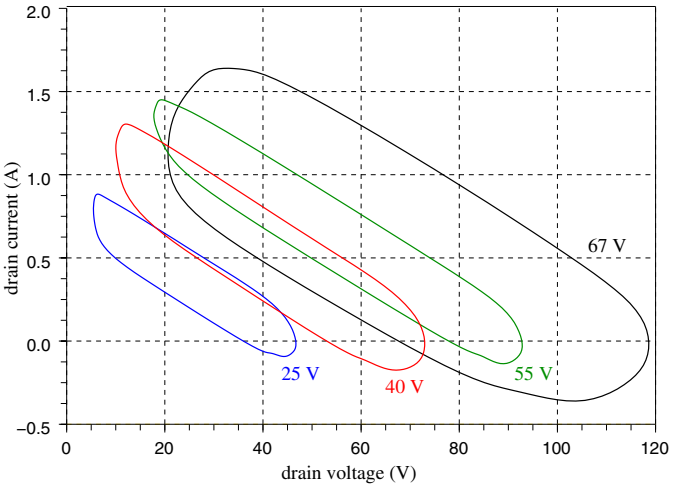

Fig.7 Load lines corresponding to the couples (Pout, Pin) of Fig 6: 25V (blue), 40V (red), 55V (green) and 67V (black).